



# OSRAM

*Slimline*

STANDARD RED **SCD5580A**

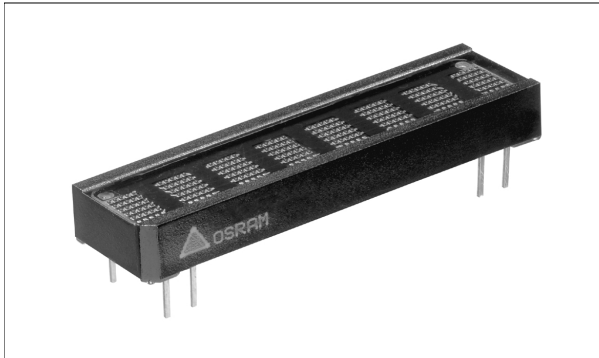
YELLOW **SCD5581A**

HIGH EFFICIENCY RED **SCD5582A**

GREEN **SCD5583A**

HIGH EFFICIENCY GREEN **SCD5584A**

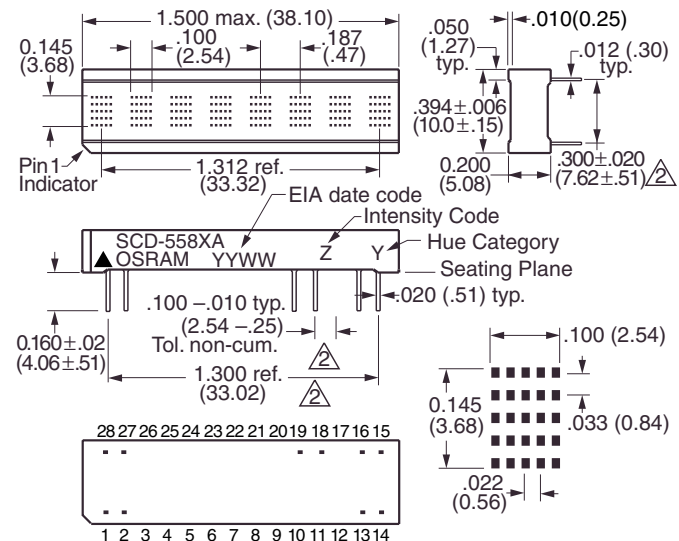
**0.145" 8-Character 5 x 5 Dot Matrix Serial Input  
Dot Addressable Intelligent Display® Devices**



## FEATURES

- **Low Profile Package: 60% Smaller than Industry Standard 8-Digit Display**
- **Eight 0.145" (3.68 mm) 5 x 5 Dot Matrix Characters in Red, Yellow, High Efficiency Red, Green, or High Efficiency Green**
- **Optimum Display Surface Efficiency (display area to package ratio)**
- **Low Power—30% Less Power Dissipation than 5 x 7 Format**
- **High Speed Data Input Rate: 5.0 MHz**
- **ROMless Serial Input, Dot Addressable Display—Ideal for User Defined Characters**
- **Built-in Decoders, Multiplexers and LED Drivers**
- **Readable from 6.0 feet (1.8 meters)**
- **Wide Viewing Angle, X Axis  $\pm 55^\circ$ , Y Axis  $\pm 65^\circ$**
- **Attributes:**
  - **200 Bit RAM for User Defined Characters**
  - **Eight Dimming Levels**
  - **Power Down Mode (<250  $\mu$ W)**
  - **Hardware/Software Clear Function**
  - **Lamp Test**
- **Internal or External Clock**
- **End-Stackable Dual-In-Line Plastic Package**
- **3.3 V Capability**

Dimensions in inches (mm)



Notes: Unless otherwise specified

1. Tolerances .XXX  $\pm$  0.10(0.254)
2. Dimension at seating plane
3. Lead Dim. 0.018 wide x 0.012 thk.

## DESCRIPTION

The SCD5580A (Red), SCD5581A (Yellow), SCD5582A (HER), SCD5583A (Green) and SCD5584A (HEG) are eight digit dot addressable 5 x 5 matrix, Serial Input, Intelligent Display devices. The eight 0.145" (3.68 mm) high digits are packaged in a transparent, 0.3" pin spacing plastic DIP.

The on-board CMOS has a 200 bit RAM, (one bit associated with one LED), to generate User Defined Characters. Due to the reduced LED count, power requirement and heat dissipation are reduced by 30%. Additionally in Power Down Mode quiescent current is <50  $\mu$ A.

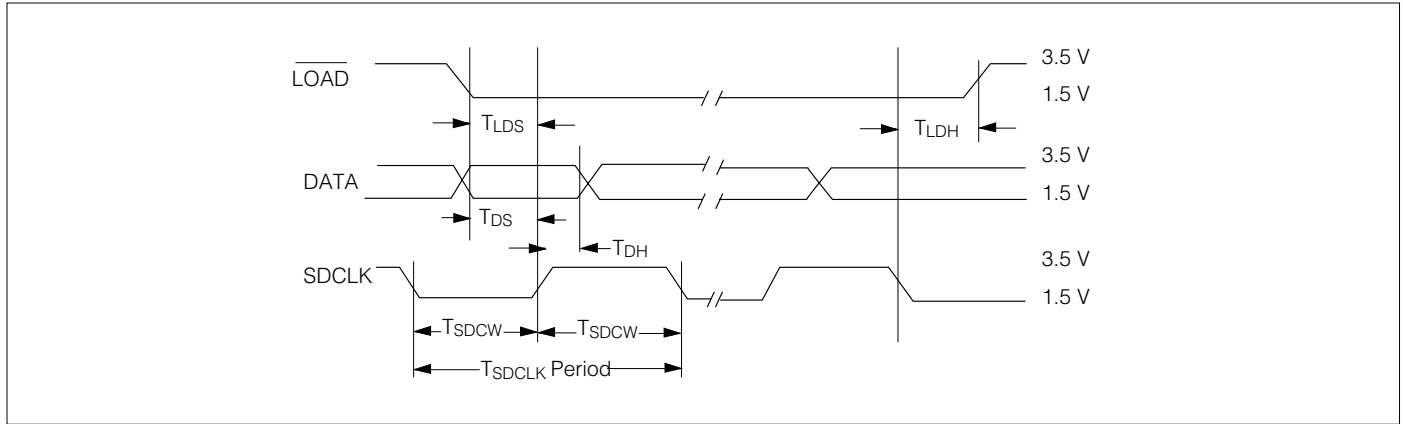
**DESCRIPTION** (continued)

The SCD558XA is designed to work with the Serial port of most common microprocessors. The Clock I/O (CLK I/O) and Clock Select ( $\overline{\text{CLKSEL}}$ ) pins offer the user the capability to supply a high speed external clock. This feature can minimize audio band interference for portable communication equipment or eliminate the visual synchronization effects found in high vibration environments such as avionics equipment.

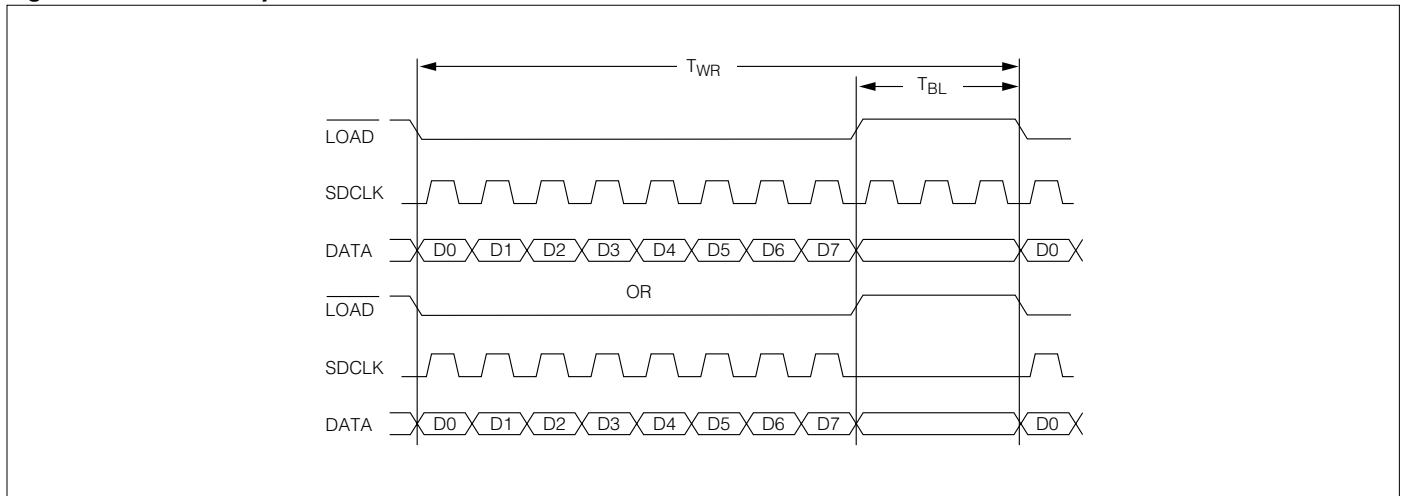
**Maximum Ratings**

DC Supply Voltage .....	-0.5 to +7.0 Vdc
Input Voltage Levels Relative to Ground .....	-0.5 to $V_{CC} + 0.5$ Vdc
Operating Temperature .....	-40°C to +85°C
Storage Temperature .....	-40°C to +100°C
Maximum Solder Temperature	
0.063" below Seating Plane, $t < 5$ s .....	260°C
Relative Humidity at 85°C .....	85%
Maximum Number of LEDs on at 100% Brightness .....	128
IC Junction Temperature .....	125°C
ESD (100 pF, 1.5 k $\Omega$ ) .....	2.0 kV
Max SDCLK frequency .....	5.0 MHz

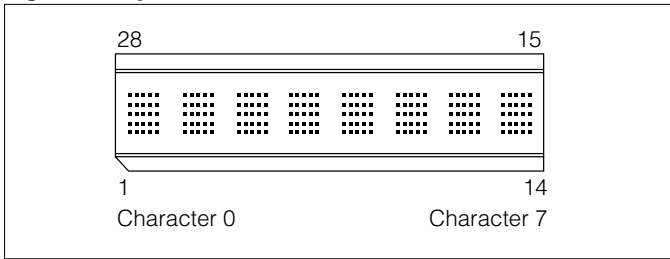
**Figure 1. Data Write Cycle**



**Figure 2. Instruction Cycle**



**Figure 3. Top View**



**Electrical Characteristics at 25°C**

Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CC}$	4.5	5.0	5.5	V	—
$I_{CC}$ (Pwr Dwn Mode) <sup>(1)(2)</sup>	—	5.0	—	$\mu$ A	$V_{CC}=5.0$ V, all inputs=0 V or $V_{CC}$
$I_{CC}$ 8 digits <sup>(3)</sup> 16 dots/character	—	200	240	mA	$V_{CC}=5.0$ V, “#” displayed in all 8 digits at 100% brightness at 25°C
$I_{IL}$ Input current	—	—	-10	$\mu$ A	$V_{CC}=5.0$ V, $V_{IN}=0$ (all inputs)
$I_{IH}$ Input current	—	—	10	$\mu$ A	$V_{CC}=V_{IN}=5.0$ V (all inputs)
$V_{IH}$	3.5	—	—	V	$V_{CC}=4.5$ V to 5.5 V
$V_{IL}$	—	—	1.5	V	$V_{CC}=4.5$ V to 5.5 V
$I_{OH}$ (CLK I/O)	—	-8.9	—	mA	$V_{CC}=4.5$ V, $V_{OH}=2.4$ V
$I_{OL}$ (CLK I/O)	—	1.6	—	mA	$V_{CC}=4.5$ V, $V_{OL}=0.4$ V
$\theta_{J-pin}$	—	35	—	°C/W	—
$F_{ext}$ External Clock Input Frequency	120	—	347	kHz	$V_{CC}=5.0$ V, $\overline{CLKSEL}=0$
$F_{osc}$ Internal Clock Input Frequency	120	—	347	kHz	$V_{CC}=5.0$ V, $\overline{CLKSEL}=1.0$
Clock I/O Bus Loading	—	—	240	pF	—
Clock Out Rise Time	—	—	500	ns	$V_{CC}=4.5$ V, $V_{OH}=2.4$ V
Clock Out Fall Time	—	—	500	ns	$V_{CC}=4.5$ V, $V_{OH}=0.4$ V
Digit Multiplex Frequency	375	768	1086	Hz	—

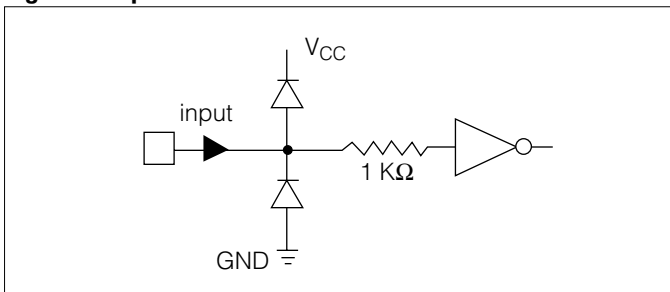
**Notes:**

- 1) When an external clock is used it must be stopped.
- 2) Unused inputs must be tied high.
- 3) Peak current  $^{5/3} \times I_{CC}$ .

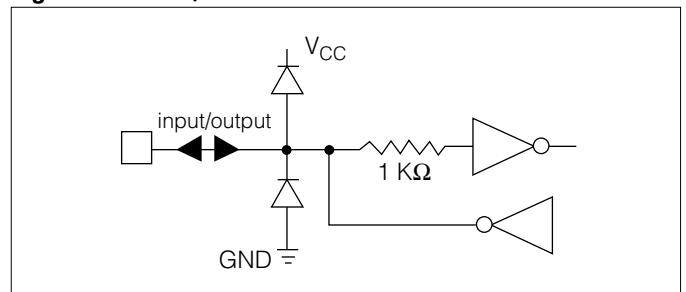
**Input/Output Circuits**

Figures 5 and 6 show the input and output resistor/diode networks used for ESD protection and to eliminate substrate latch-up caused by input voltage over/under shoot.

**Figure 4. Inputs**



**Figure 5. Clock I/O**



## Optical Characteristics at 25°C

( $V_{CC}=5.0$  V at 100% brightness level, viewing angle: X axis  $\pm 55^\circ$ , Y axis  $\pm 65^\circ$ )

### Red SCD5580A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	$I_V$	36	90	$\mu\text{cd/dot}$
Peak Wavelength	$\lambda_{\text{peak}}$	—	660	nm
Dominant Wavelength	$\lambda_{\text{dom}}$	—	639	nm

### Yellow SCD5581A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	$I_V$	124	213	$\mu\text{cd/dot}$
Peak Wavelength	$\lambda_{\text{peak}}$	—	583	nm
Dominant Wavelength	$\lambda_{\text{dom}}$	—	585	nm

### High Efficiency Red SCD5582A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	$I_V$	124	265	$\mu\text{cd/dot}$
Peak Wavelength	$\lambda_{\text{peak}}$	—	630	nm
Dominant Wavelength	$\lambda_{\text{dom}}$	—	626	nm

### Green SCD5583A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	$I_V$	124	221	$\mu\text{cd/dot}$
Peak Wavelength	$\lambda_{\text{peak}}$	—	565	nm
Dominant Wavelength	$\lambda_{\text{dom}}$	—	570	nm

### High Efficiency Green SCD5584A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	$I_V$	124	505	$\mu\text{cd/dot}$
Peak Wavelength	$\lambda_{\text{peak}}$	—	568	nm
Dominant Wavelength	$\lambda_{\text{dom}}$	—	574	nm

#### Notes:

1. Dot to dot intensity matching at 100% brightness is 1.8:1.
2. Displays are binned for hue at 2.0 nm intervals.
3. Displays within a given intensity category have an intensity matching of 1.5:1 (max.).

### Pin Assignment

Pin	Function	Pin	Function
1	SDCLK	28	GND
2	$\overline{\text{LOAD}}$	27	DATA
3	NP	26	NP
4	NP	25	NP
5	NP	24	NP
6	NP	23	NP
7	NP	22	NP
8	NP	21	NP
9	NP	20	NP
10	NP	19	V <sub>CC</sub>
11	NP	18	NC
12	NP	17	NP
13	$\overline{\text{RST}}$	16	$\overline{\text{CLKSEL}}$
14	GND	15	CLK I/O

### Switching Specifications

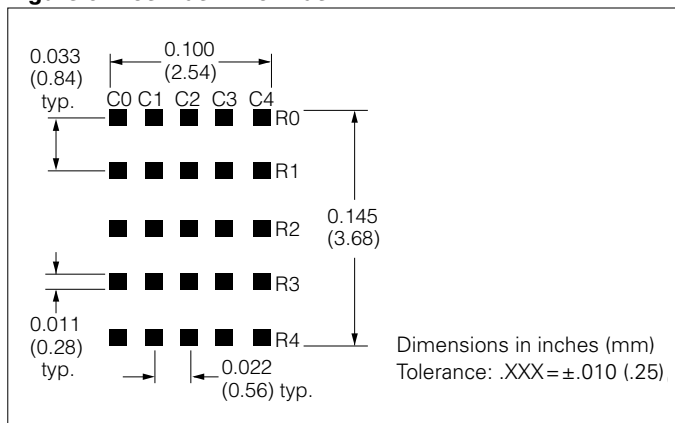
(T<sub>A</sub>=25°C and V<sub>CC</sub>=4.5 V to 5.5 V)

Symbol	Description	Min.	Units
T <sub>RC</sub>	Reset Active Time	600	ns
T <sub>LDS</sub>	Load Setup Time	40	ns
T <sub>DS</sub>	Data Setup Time	40	ns
T <sub>SDCLK</sub>	Clock Period	200	ns
T <sub>SDCW</sub>	Clock Width	70	ns
T <sub>LDH</sub>	Load Hold Time	0	ns
T <sub>DH</sub>	Data Hold Time	20	ns
T <sub>WR</sub>	Total Write Time	2.2	μs
T <sub>BL</sub>	Time Between Loads	600	ns

#### Note:

SDCLK duty cycle=30% Min. and 50% Max.

Figure 6. Dot Matrix Format



### Pin Definitions

Pin	Function	Definitions
1	SDCLK	Loads data into the 8-bit serial data register on a low to high transition.
2	$\overline{\text{LOAD}}$	Low input enables data clocking into 8-bit serial shift register. When LOAD goes high, the contents of 8-bit serial Shift Register will be decoded.
3	NP	No pin
4	NP	No pin
5	NP	No pin
6	NP	No pin
7	NP	No pin
8	NP	No pin
9	NP	No pin
10	NP	No pin
11	NP	No pin
12	NP	No pin
13	$\overline{\text{RST}}$	Asynchronous input, when low will clear the Multiplex Counter, User RAM and Data Register. Control Word Register is set to 100% brightness and the Address Register is set to select Digit 0. The display is blanked.
14	GND	Power supply ground
15	CLK I/O	Outputs master clock or inputs external clock.
16	$\overline{\text{CLKSEL}}$	H=internal clock, L=external clock
17	NP	No pin
18	NC	No connection
19	V <sub>CC</sub>	Power supply
20	NP	No pin
21	NP	No pin
22	NP	No pin
23	NP	No pin
24	NP	No pin
25	NP	No pin
26	NP	No pin
27	DATA	Serial data input
28	GND	Power supply ground

### Display Column and Row Format

	C0	C1	C2	C3	C4
Row 0	1	1	1	1	1
Row 1	0	0	1	0	0
Row 2	0	0	1	0	0
Row 3	0	0	1	0	0
Row 4	0	0	1	0	0

1=Display dot "On"  
0=Display dot "Off"

### Column Data Ranges

Row 0	00H to 1FH
Row 1	20H to 3FH
Row 2	40H to 5FH
Row 3	60H to 7FH
Row 4	80H to 9FH

### Operation of the SCD558XA

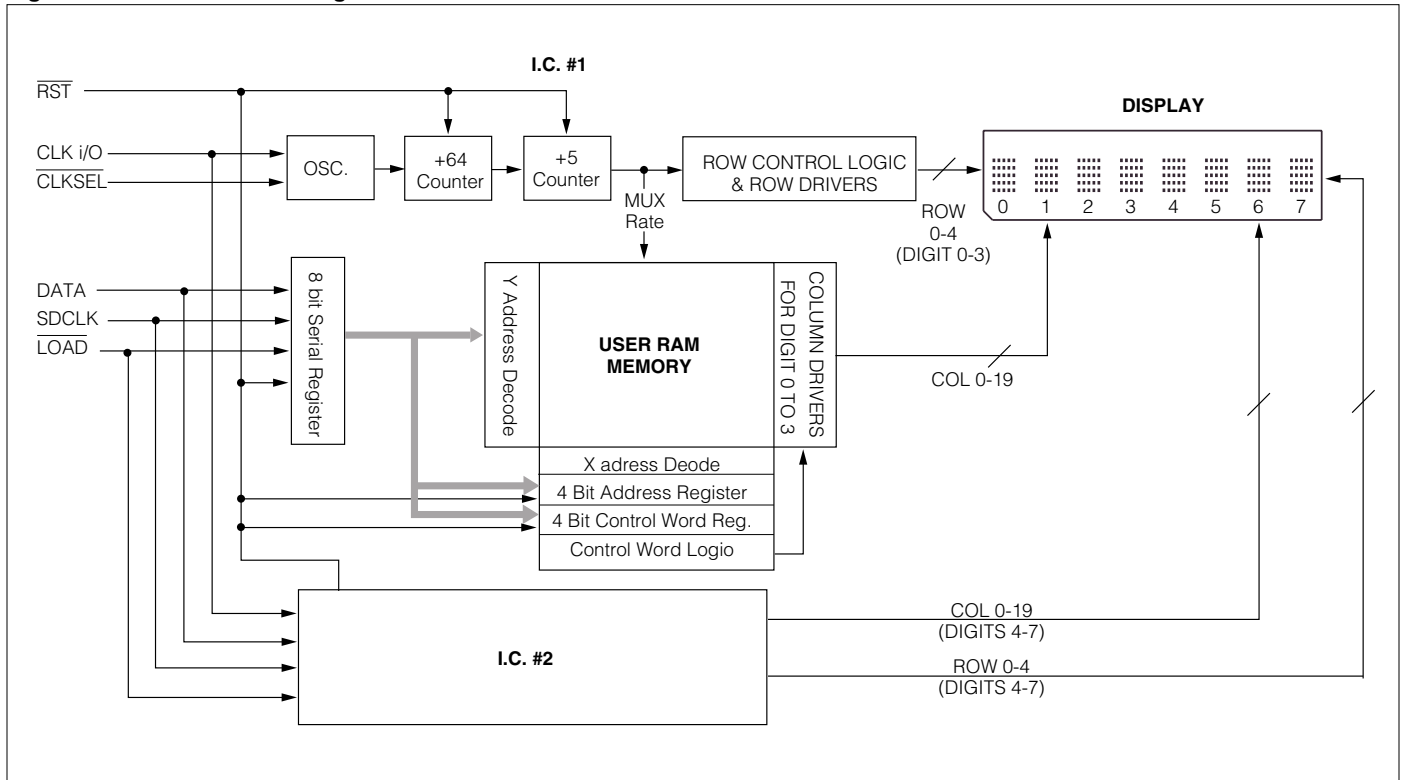
The display consists of 2 CMOS ICs containing control logic and drivers for eight 5 x 5 characters. These components are assembled in a compact (38 mm x 10 mm) plastic package.

Individual LED dot addressability allows the user great freedom in creating special characters or mini-icons. The User Definable Character Set Examples illustrate 200 different character and symbol possibilities.

The use of a serial data interface provides a highly efficient interconnection between the display and the mother board. The SCD558XA requires only 4 lines as compared to 15 for an equivalent 8 character parallel input part.

The on-board CMOS ICs are the electronic heart of the display. The IC accepts decoded serial data, which is stored in the internal RAM. Asynchronously the RAM is read by the character multiplexer at a strobe rate that results in a flicker free display. Figure 7 shows the three functional areas of the ICs. These include: the input serial data register and control logic, a 200 bits two port RAM, and an internal multiplexer/display driver.

Figure 7. SCD558X Block Diagram



The following explains how to format the serial data to be loaded into the display. The user supplies a string of bit mapped decoded characters. The contents of this string is shown in Figure 8a. Figure 8b shows that each character consists of six 8 bit words. The first word encodes the display character location and the succeeding five bytes are row data. The row data represents the status (On, Off) of individual column LEDs. Figure 9c shows that each 8 bit word is formatted to include a three bit Operational Code (OPCODE) defined by bits D7–D5 and five bits (D4–D0) representing Column Data, Character Address, or Control Word Data.

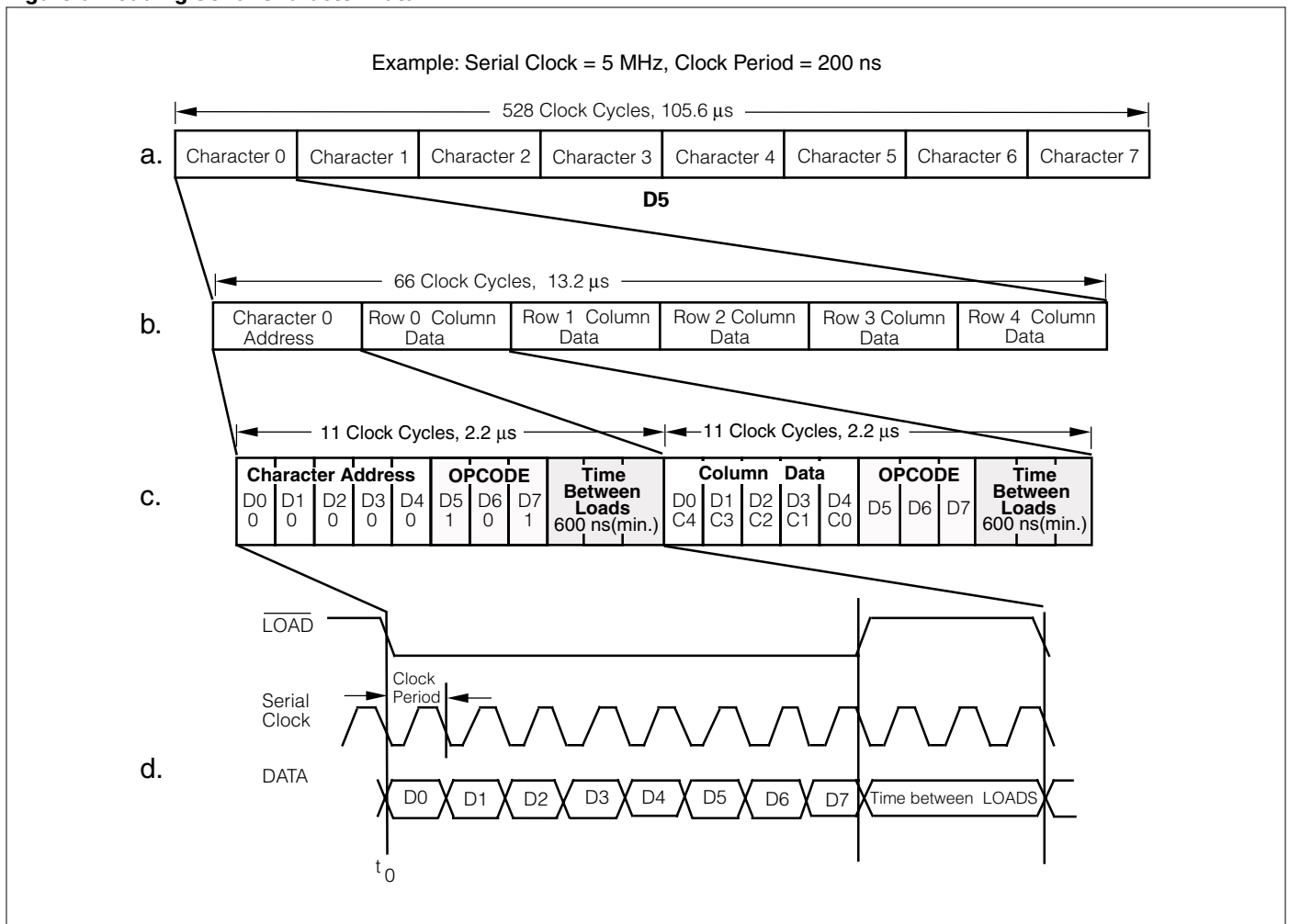
Figure 8d shows the sequence for loading the bytes of data. Bringing the  $\overline{\text{LOAD}}$  line low enables the serial register to accept data. The shift action occurs on the low to high transition of the serial data clock (SDCLK). The least significant bit (D0) is loaded first. After eight clock pulses the  $\overline{\text{LOAD}}$  line is brought high. With this transition the OPCODE is decoded. The decoded OPCODE directs D4–D0 to be latched in the Character Address register, stored in the RAM as Column data, or latched in the Control Word register. The control IC requires a minimum 600 ns delay between successive byte loads. As indicated in Figure 8a, a total of 528 bits of data are required to load all eight characters into the display.

The Character Address Register bits, D4–D0 (Table 2), and Row Address Register bits, D7–D5 (Table 3), direct the Column Data bits, D4–D0 (Table 3) to specific RAM location. Table 1 shows the Row Address for the example character "D." Column data is written and read asynchronously from the 200 bit RAM. Once loaded the internal oscillator and character multiplexer reads the data from the RAM. These characters are row strobed with column data as shown in Figures 10 and 11. The character strobe rate is determined by the internal or user supplied external MUX Clock and the IC's  $\div 320$  counter.

**Table 1. Character "D"**

	Op code			Column Data					Hex
	D7	D6	D5	D4	D3	D2	D1	D0	
	C0	C1	C2	C3	C4				
Row 0	0	0	0	1	1	1	1	0	1E
Row 1	0	0	1	1	0	0	0	1	31
Row 2	0	1	0	1	0	0	0	1	51
Row 3	0	1	1	1	0	0	0	1	71
Row 4	1	0	0	1	1	1	1	0	9E

**Figure 8. Loading Serial Character Data**



**Table 2. Load Character Address**

Op code D7 D6 D5	Character Address D4 D3 D2 D1 D0	Hex	Operation Load
1 0 1	0 0 0 0 0	A0	Character 0
1 0 1	0 0 0 0 1	A1	Character 1
1 0 1	0 0 0 1 0	A2	Character 2
1 0 1	0 0 0 1 1	A3	Character 3
1 0 1	0 0 1 0 0	A4	Character 4
1 0 1	0 0 1 0 1	A5	Character 5
1 0 1	0 0 1 1 0	A6	Character 6
1 0 1	0 0 1 1 1	A7	Character 7

**Table 3. Load Column Data**

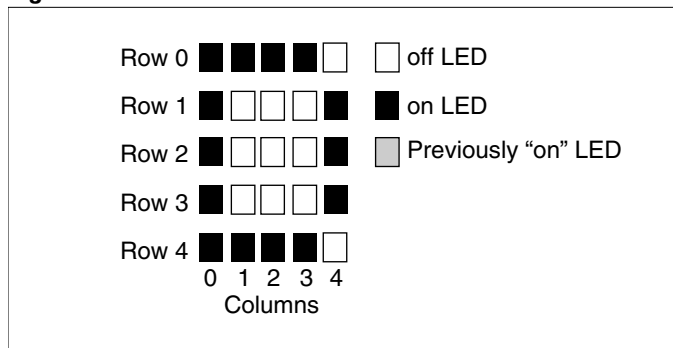
Op code D7 D6 D5	Column Data D4 D3 D2 D1 D0	Operation Load
0 0 0	C0 C1 C2 C3 C4	Row 0
0 0 1	C0 C1 C2 C3 C4	Row 1
0 1 0	C0 C1 C2 C3 C4	Row 2
0 1 1	C0 C1 C2 C3 C4	Row 3
1 0 0	C0 C1 C2 C3 C4	Row 4

The user can activate four Control functions. These include: LED Brightness Level, Lamp Test, IC Power Down, or Display Clear. OPCODEs and five bit words are used to initiate these functions. The OPCODEs and Control Words for the Character Address and Loading Column Data are shown in Tables 2 and 3.

The user can select seven specific LED brightness levels, Table 4. These brightness levels (in percentages of full brightness of the display) include: 100% (F0<sub>HEX</sub>), 53% (F1<sub>HEX</sub>), 40% (F2<sub>HEX</sub>), 27% (F3<sub>HEX</sub>), 20% (F4<sub>HEX</sub>), 13% (F5<sub>HEX</sub>), and 6.6% (F6<sub>HEX</sub>). The brightness levels are controlled by changing the duty factor of the row strobe pulse.

The SCD558XA offers a unique Display Power Down feature which reduces  $I_{CC}$  to less than 50  $\mu$ A. When FF<sub>HEX</sub> is loaded, as shown in Table 5, the display is set to 0% brightness and the internal multiplex clock is stopped. When in the Power Down mode data may still be written into the RAM. The display is reactivated by loading a new Brightness Level Control Word into the display.

**Figure 9. Row and Column Location**



**Table 4. Display Brightness**

Op code D7 D6 D5	Control Word D4 D3 D2 D1 D0	Hex	Operation Level
1 1 1	1 0 0 0 0	F0	100%
1 1 1	1 0 0 0 1	F1	53%
1 1 1	1 0 0 1 0	F2	40%
1 1 1	1 0 0 1 1	F3	27%
1 1 1	1 0 1 0 0	F4	20%
1 1 1	1 0 1 0 1	F5	13%
1 1 1	1 0 1 1 0	F6	6.6%

**Table 5. Power Down**

Op code D7 D6 D5	Control Word D4 D3 D2 D1 D0	Hex	Operation Level
1 1 1	1 1 1 1 1	FF	0% brightness

The Lamp Test is enabled by loading F8<sub>HEX</sub>, Table 6, into the serial shift register. This Control Word sets all of the LEDs to a 53% brightness level. Operation of the Lamp Test has no affect on the RAM and is cleared by loading a Brightness Control Word.

**Table 6. Lamp Test**

Op code D7 D6 D5	Control Word D4 D3 D2 D1 D0	Hex	Operation Level
1 1 1	1 0 B B B		Lamp Test (OFF)
1 1 1	1 1 0 0 0	F8	Lamp Test (ON)

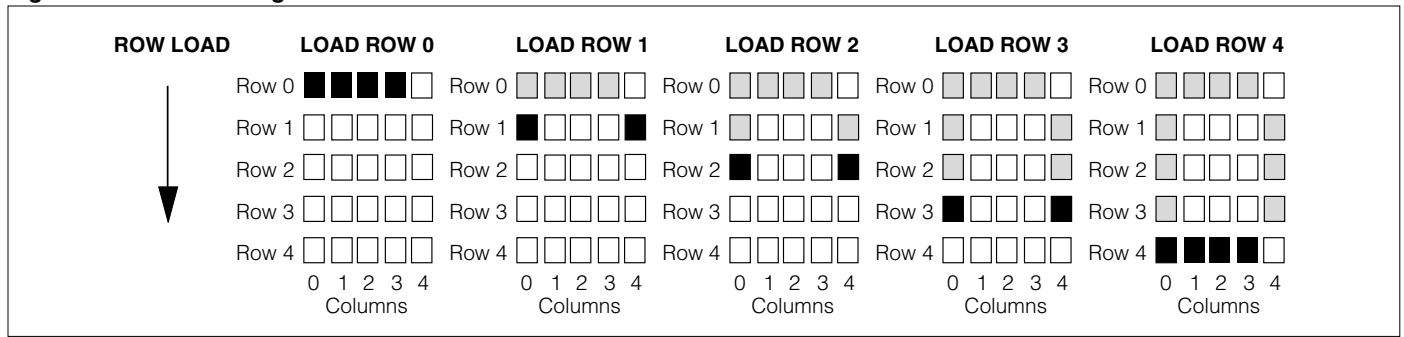
The Software Clear (C0<sub>HEX</sub>), given in Table 7, clears the Address Register and the RAM. The display is blanked and the Character Address Register will be set to Character 0. The internal counter and the Control Word Register are unaffected. The Software Clear will remain active until the next data input cycle is initiated.

**Table 7. Software Clear**

Op code D7 D6 D5	Control Word D4 D3 D2 D1 D0	Hex	Operation Level
1 1 0	0 0 0 0 0	C0	CLEAR



**Figure 10. Row Strobing**



**Multiplexer and Display Driver**

The eight characters are row multiplexed with RAM resident column data. The strobe rate is established by the internal or external MUX Clock rate. The MUX Clock frequency is divided by a 320 counter chain. This results in a typical strobe rate of 750 Hz. By pulling the Clock SEL line low, the display can be operated from an external MUX Clock. The external clock is attached to the CLK I/O connection (pin 15). The maximum external MUX Clock frequency should be limited to 1.0 MHz.

An asynchronous hardware Reset (pin 13) is also provided. Bringing this pin low will clear the Character Address Register, Control Word Register, RAM, and blanks the display. This action leaves the display set at Character Address 0, and the Brightness Level set at 100%.

**Thermal Considerations**

The SCD558XA has been designed to provide lowest thermal resistance from the CMOS to the ground pin.

The heat is then conducted through the traces on the users circuit board to free air. The max. IC operating temperature is 125°C. Maximum IC junction temperature is calculated using the following equation:

$$T_J \text{ (IC) Max.} = T_A + (P_D \text{ Max.}) (R_{\theta J-PIN} + R_{\theta PIN-A})$$

where  $R_{\theta J-PIN} = 35^\circ\text{C/W}$ .

$$P_D \text{ Max.} = V_{CC} \text{ Max.} \times I_{CC} \text{ Max.} = 5.5 \text{ V} \times 0.240 = 1.32 \text{ W.}$$

$R_{\theta PIN-A}$  will depend on ground trace thickness, whether parts are soldered to the pcb or socketed and on air circulation.

**Electrical & Mechanical Considerations**

**Interconnect Considerations**

Optimum product performance can be had when the following electrical and mechanical recommendations are adopted. The SCD558XA's ICs are constructed in a high speed CMOS process, consequently high speed noise on the SERIAL DATA, SERIAL DATA CLOCK,  $\overline{\text{LOAD}}$  and  $\overline{\text{RESET}}$  lines may cause incorrect data to be written into the serial shift register. Adhere to transmission line termination procedures when using fast line drivers and long cables (>10 cm).

Good digital grounds (pins 14, 28) and power supply decoupling (pins 6, 9, 20, 23) will insure that  $I_{CC}$  (<400 mA peak) switching currents do not generate localized ground bounce. Therefore it is recommended that each display package use a 0.1  $\mu\text{F}$  and 20  $\mu\text{F}$  capacitor between  $V_{CC}$  and ground.

When the internal MUX Clock is being used, connect the  $\overline{\text{CLKSEL}}$  pin to  $V_{CC}$  and leave CLK I/O floating. In those applica-

tions where  $\overline{\text{RESET}}$  will not be connected to the system's reset control, it is recommended that this pin be connected to the center node of a series 0.1,  $\mu\text{F}$  and 100 k $\Omega$  RC network. Thus upon initial power up the  $\overline{\text{RESET}}$  will be held low for 10 ms allowing adequate time for the system power supply to stabilize.

**ESD Protection**

The input protection structure of the SCD558XA provides significant protection against ESD damage. It is capable of withstanding discharges greater than 2.0 kV. Take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

**Soldering Considerations**

The SCD558XA can be hand soldered with SN63 solder using a grounded iron set to 260°C.

Wave soldering is also possible following these conditions: Pre-heat that does not exceed 93°C on the solder side of the PC board or a package surface temperature of 85°C. Water soluble organic acid flux (except carboxylic acid) or rosin-based RMA flux without alcohol can be used.

Wave temperature of 245°C  $\pm$ 5°C with a dwell between 1.5 sec. to 3.0 sec. Exposure to the wave should not exceed temperatures above 260°C for five seconds at 0.063" below the seating plane. The packages should not be immersed in the wave.

**Post Solder Cleaning Procedures**

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the nylon package. Maximum exposure should not exceed two minutes at elevated temperatures. Acceptable solvents are TF (trichlorotrifluoroethane), TA, 111 Trichloroethane, and unheated acetone. <sup>(1)</sup>

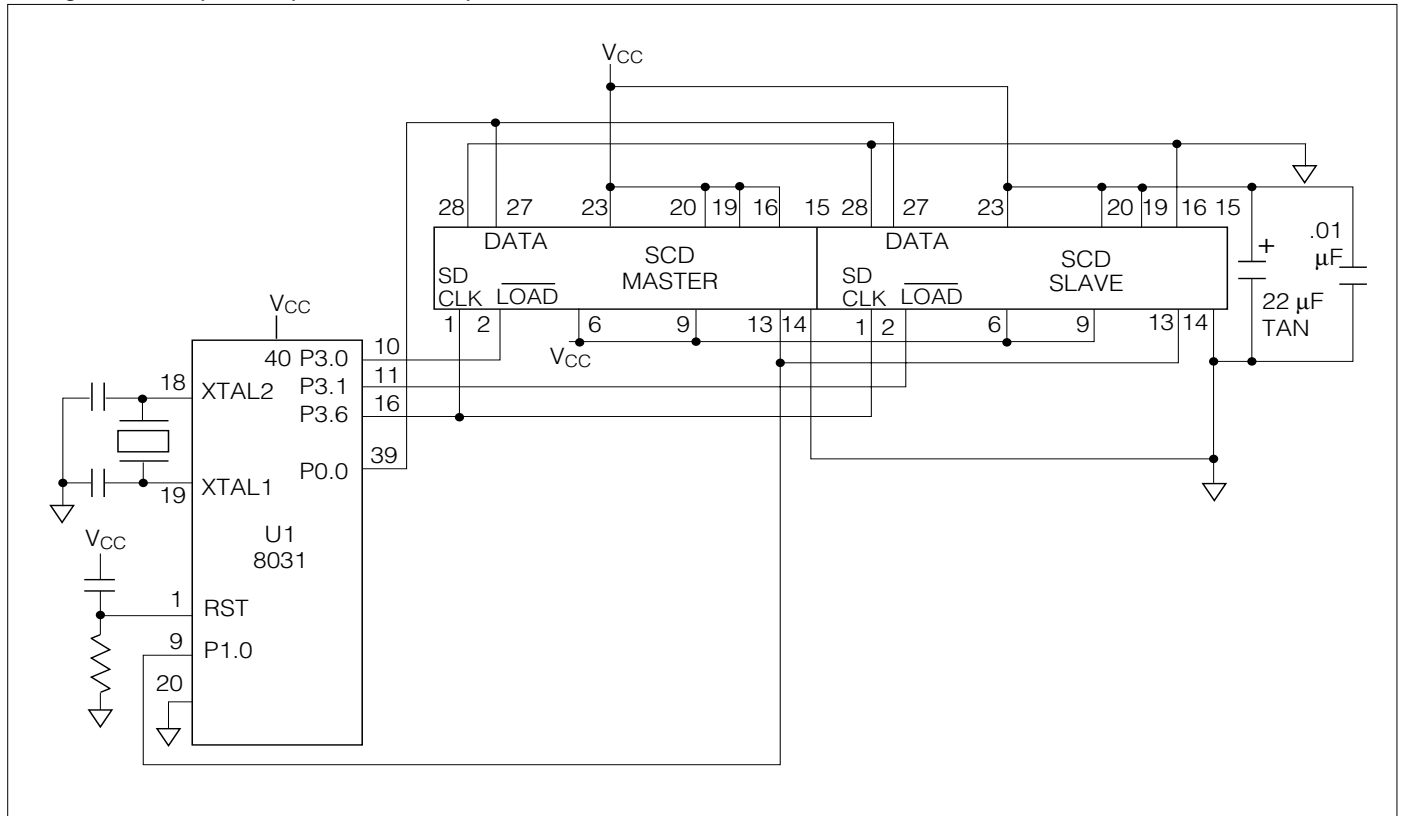
**Note:**

<sup>1)</sup> Acceptable commercial solvents are: Basic TF, Arklone, P. Genesolv, D. Genesolv DA, Blaco-Tron TF, Blaco-Tron TA, and Freon TA.

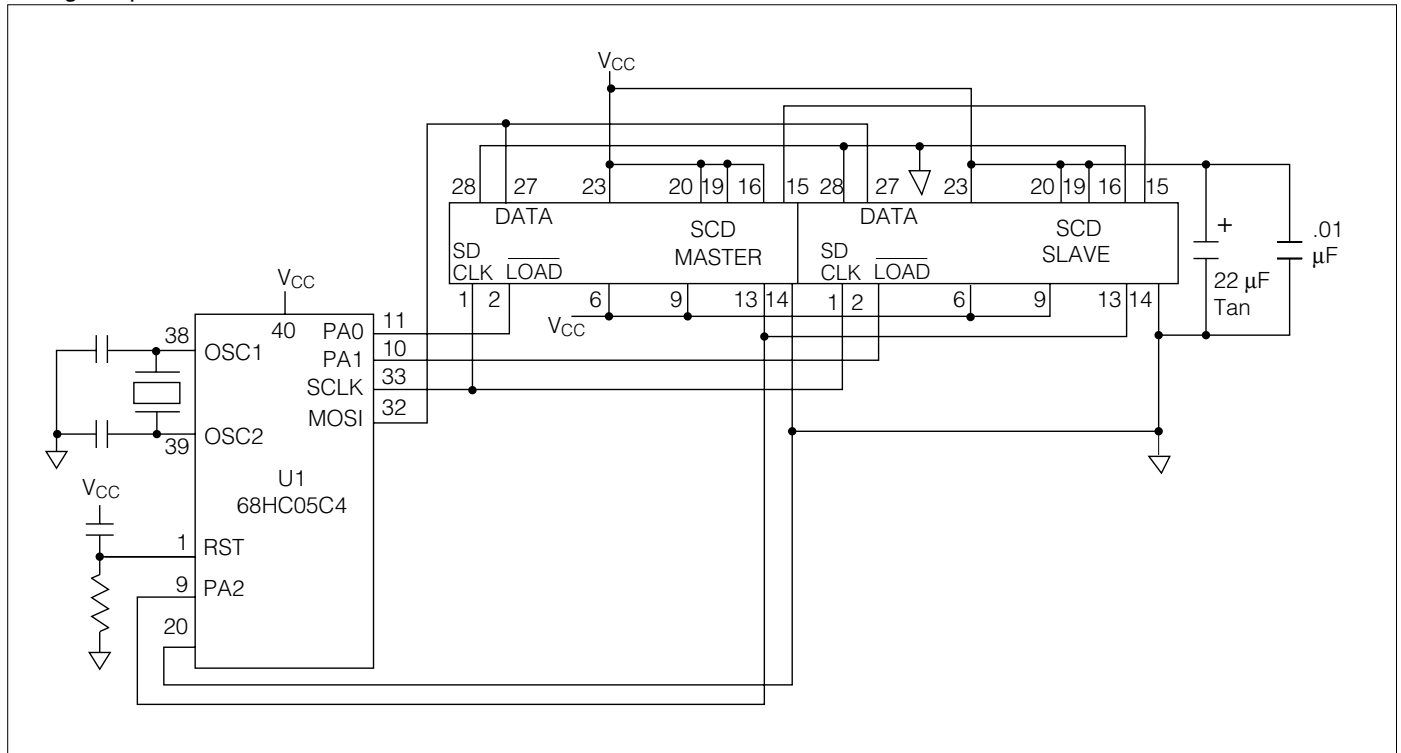
Unacceptable solvents contain alcohol, methanol, methylene chloride, ethanol, TP35, TCM, TMC, TMS+, TE, or TES. Since many commercial mixtures exist, contact a solvent vendor for chemical composition information. Some major solvent manufacturers are: Allied Chemical Corporation, Specialty Chemical



**Figure 12. Interface with Siemens/Intel 8031 Microprocessor**  
(using one bit of parallel port as serial input)



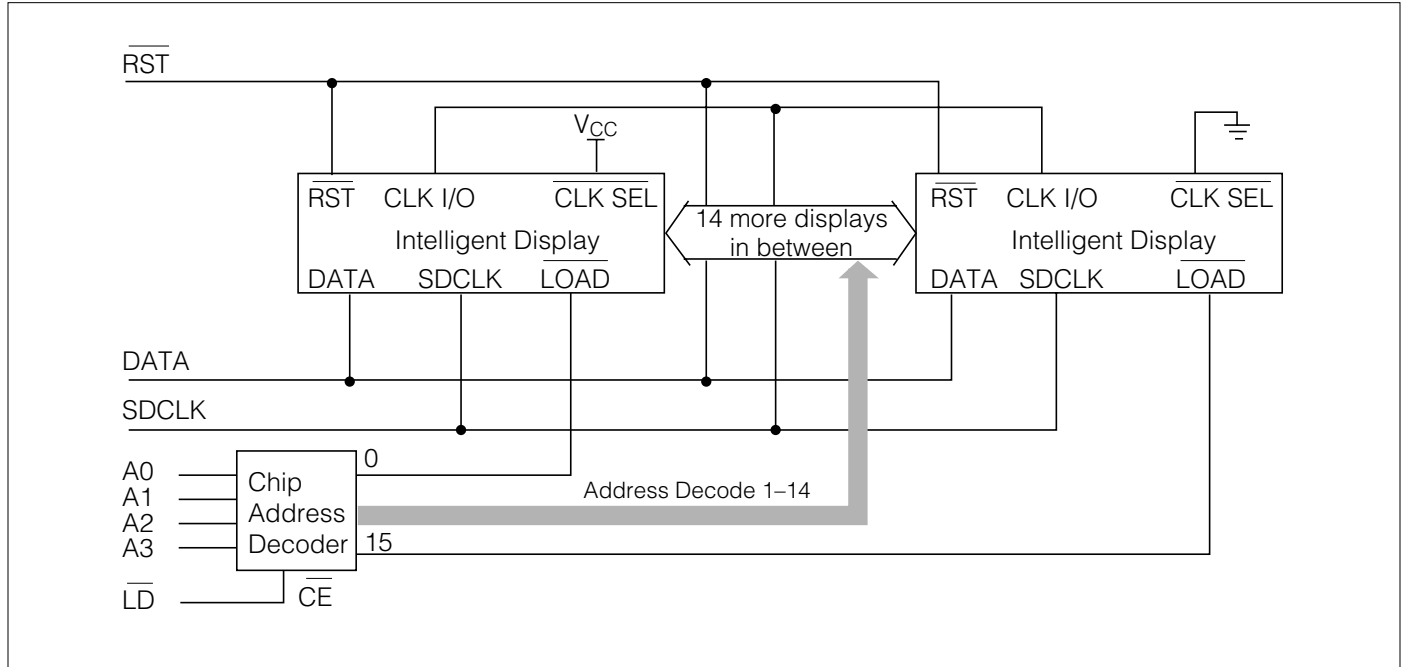
**Figure 13. Interface with Motorola 68HC05C4 Microprocessor**  
(using SPI port)



## Cascading Multiple Displays

Multiple displays can be cascaded using the  $\overline{\text{CLK SEL}}$  and CLK I/O pins as shown below. The display designated as the Master Clock source should have its  $\overline{\text{CLK SEL}}$  pin tied high and the slaves should have their  $\overline{\text{CLK SEL}}$  pins tied low. All CLK I/O pins should be tied together. One display CLK I/O can drive 15 slave CLK I/Os. Use  $\overline{\text{RST}}$  to synchronize all display counters.

**Figure 14. Cascading Multiple Displays**



## Loading Data Into the Display

Use following procedure to load data into the display:

1. Power up the display.
2. Bring  $\overline{\text{RST}}$  low (600 ns duration minimum) to clear the Multiplex Counter, Address Register, Control Word Register, User RAM and Data Register. The display will be blank. Display brightness is set to 100%.
3. If a different brightness is desired, load the proper brightness opcode into the Control Word Register.
4. Load the Digit Address into the display.
5. Load display row and column data for the selected digit.
6. Repeat steps 4 and 5 for all digits.

### Data Contents for the Word "Displays"

Step	D7	D6	D5	D4	D3	D2	D1	D0	Function
A	1	1	0	0	0	0	0	0	CLEAR
B (optional)	1	1	1	1	0	B	B	B	BRIGHTNESS SELECT
1	1	0	1	0	0	0	0	0	DIGIT D0 SELECT
2	0	0	0	1	1	1	1	0	ROW 0 D0 (D)
3	0	0	1	1	0	0	0	1	ROW 1 D0 (D)
4	0	1	0	1	0	0	0	1	ROW 2 D0 (D)
5	0	1	1	1	0	0	0	1	ROW 3 D0 (D)
6	1	0	0	1	1	1	1	0	ROW 4 D0 (D)
7	1	0	1	0	0	0	0	1	DIGIT D1 (I)
8	0	0	0	0	1	1	1	0	ROW 0 D1 (I)
9	0	0	1	0	0	1	0	0	ROW 1 D1 (I)
10	0	1	0	0	0	1	0	0	ROW 2 D1 (I)
11	0	1	1	0	0	1	0	0	ROW 3 D1 (I)
12	1	0	0	0	1	1	1	0	ROW 4 D1 (I)
13	1	0	1	0	0	0	1	0	DIGIT D2 (S)
14	0	0	0	0	1	1	1	1	ROW 0 D2 (S)
15	0	0	1	1	0	0	0	0	ROW 1 D2 (S)
16	0	1	0	0	1	1	1	0	ROW 2 D2 (S)
17	0	1	1	0	0	0	0	1	ROW 3 D2 (S)
18	1	0	0	1	1	1	1	0	ROW 4 D2 (S)
19	1	0	1	0	0	0	1	1	DIGIT D3 (P)
20	0	0	0	1	1	1	1	0	ROW 0 D3 (P)
21	0	0	1	1	0	0	0	1	ROW 1 D3 (P)
22	0	1	0	1	1	1	1	0	ROW 2 D3 (P)
23	0	1	1	1	0	0	0	0	ROW 3 D3 (P)
24	1	0	0	1	0	0	0	0	ROW 4 D3 (P)
25	1	0	1	0	0	1	0	0	DIGIT D4 (L)
26	0	0	0	1	0	0	0	0	ROW 0 D4 (L)
27	0	0	1	1	0	0	0	0	ROW 1 D4 (L)
28	0	1	0	1	0	0	0	0	ROW 2 D4 (L)
29	0	1	1	1	0	0	0	0	ROW 3 D4 (L)
30	1	0	0	1	1	1	1	1	ROW 4 D4 (L)
31	1	0	1	0	0	1	0	1	DIGIT D5 (A)
32	0	0	0	0	0	1	0	0	ROW 0 D5 (A)
33	0	0	1	0	1	0	1	0	ROW 1 D5 (A)
34	0	1	0	1	1	1	1	1	ROW 2 D5 (A)
35	0	1	1	1	0	0	0	1	ROW 3 D5 (A)
36	1	0	0	1	0	0	0	1	ROW 4 D5 (A)
37	1	0	1	0	0	1	1	0	DIGIT D6 (Y)
38	0	0	0	1	0	0	0	1	ROW 0 D6 (Y)
39	0	0	1	0	1	0	1	0	ROW 1 D6 (Y)
40	0	1	0	0	0	1	0	0	ROW 2 D6 (Y)
41	0	1	1	0	0	1	0	0	ROW 3 D6 (Y)
42	1	0	0	0	0	1	0	0	ROW 4 D6 (Y)
43	1	0	1	0	0	1	1	1	DIGIT D7 (S)
44	0	0	0	0	1	1	1	1	ROW 0 D7 (S)
45	0	0	1	1	0	0	0	0	ROW 1 D7 (S)
46	0	1	0	0	1	1	1	0	ROW 2 D7 (S)
47	0	1	1	0	0	0	0	1	ROW 3 D7 (S)
48	1	0	0	1	1	1	1	0	ROW 4 D7 (S)

**Note:**

If the display is already reset at Power Up, there is no need for Software Clear.

## User Definable Character Set Examples\*

### Upper and Lower Case Alphabets

HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE	
04	■	1E	■ ■ ■ ■	0F	■ ■ ■ ■	1E	■ ■ ■ ■	1F	■ ■ ■ ■	1F	■ ■ ■ ■	0F	■ ■ ■ ■	11	■ ■ ■ ■	0E	■ ■ ■ ■
2A	■ ■	29	■ ■ ■ ■	30	■ ■ ■ ■	29	■ ■ ■ ■	30	■ ■ ■ ■	30	■ ■ ■ ■	31	■ ■ ■ ■	31	■ ■ ■ ■	24	■ ■ ■ ■
5F	■ ■ ■ ■	4E	■ ■ ■ ■	50	■ ■ ■ ■	49	■ ■ ■ ■	5E	■ ■ ■ ■	5E	■ ■ ■ ■	53	■ ■ ■ ■	5F	■ ■ ■ ■	44	■ ■ ■ ■
71	■ ■ ■ ■	69	■ ■ ■ ■	70	■ ■ ■ ■	69	■ ■ ■ ■	70	■ ■ ■ ■	70	■ ■ ■ ■	71	■ ■ ■ ■	71	■ ■ ■ ■	64	■ ■ ■ ■
91	■ ■ ■ ■	9E	■ ■ ■ ■	8F	■ ■ ■ ■	9E	■ ■ ■ ■	9F	■ ■ ■ ■	90	■ ■ ■ ■	8F	■ ■ ■ ■	91	■ ■ ■ ■	8E	■ ■ ■ ■
01	■ ■ ■ ■	13	■ ■ ■ ■	10	■ ■ ■ ■	11	■ ■ ■ ■	11	■ ■ ■ ■	0E	■ ■ ■ ■	1E	■ ■ ■ ■	0C	■ ■ ■ ■	1E	■ ■ ■ ■
21	■ ■ ■ ■	34	■ ■ ■ ■	30	■ ■ ■ ■	3B	■ ■ ■ ■	39	■ ■ ■ ■	31	■ ■ ■ ■	31	■ ■ ■ ■	32	■ ■ ■ ■	31	■ ■ ■ ■
41	■ ■ ■ ■	58	■ ■ ■ ■	50	■ ■ ■ ■	55	■ ■ ■ ■	55	■ ■ ■ ■	51	■ ■ ■ ■	5E	■ ■ ■ ■	56	■ ■ ■ ■	5E	■ ■ ■ ■
71	■ ■ ■ ■	74	■ ■ ■ ■	70	■ ■ ■ ■	71	■ ■ ■ ■	73	■ ■ ■ ■	71	■ ■ ■ ■	70	■ ■ ■ ■	72	■ ■ ■ ■	74	■ ■ ■ ■
8E	■ ■ ■ ■	93	■ ■ ■ ■	9F	■ ■ ■ ■	91	■ ■ ■ ■	91	■ ■ ■ ■	8E	■ ■ ■ ■	90	■ ■ ■ ■	8D	■ ■ ■ ■	92	■ ■ ■ ■
0F	■ ■ ■ ■	1F	■ ■ ■ ■	11	■ ■ ■ ■	11	■ ■ ■ ■	11	■ ■ ■ ■	11	■ ■ ■ ■	11	■ ■ ■ ■	1F	■ ■ ■ ■		
30	■ ■ ■ ■	24	■ ■ ■ ■	31	■ ■ ■ ■	31	■ ■ ■ ■	31	■ ■ ■ ■	2A	■ ■ ■ ■	2A	■ ■ ■ ■	22	■ ■ ■ ■		
4E	■ ■ ■ ■	44	■ ■ ■ ■	51	■ ■ ■ ■	51	■ ■ ■ ■	55	■ ■ ■ ■	44	■ ■ ■ ■	44	■ ■ ■ ■	44	■ ■ ■ ■		
61	■ ■ ■ ■	64	■ ■ ■ ■	71	■ ■ ■ ■	6A	■ ■ ■ ■	7B	■ ■ ■ ■	6A	■ ■ ■ ■	64	■ ■ ■ ■	68	■ ■ ■ ■		
9E	■ ■ ■ ■	84	■ ■ ■ ■	8E	■ ■ ■ ■	84	■ ■ ■ ■	91	■ ■ ■ ■	91	■ ■ ■ ■	84	■ ■ ■ ■	9F	■ ■ ■ ■		
00	■ ■ ■ ■	10	■ ■ ■ ■	00	■ ■ ■ ■	01	■ ■ ■ ■	00	■ ■ ■ ■	04	■ ■ ■ ■	00	■ ■ ■ ■	10	■ ■ ■ ■	04	■ ■ ■ ■
2E	■ ■ ■ ■	30	■ ■ ■ ■	2F	■ ■ ■ ■	21	■ ■ ■ ■	2E	■ ■ ■ ■	2A	■ ■ ■ ■	2F	■ ■ ■ ■	30	■ ■ ■ ■	20	■ ■ ■ ■
52	■ ■ ■ ■	5E	■ ■ ■ ■	50	■ ■ ■ ■	4F	■ ■ ■ ■	5F	■ ■ ■ ■	48	■ ■ ■ ■	50	■ ■ ■ ■	56	■ ■ ■ ■	4C	■ ■ ■ ■
72	■ ■ ■ ■	71	■ ■ ■ ■	70	■ ■ ■ ■	71	■ ■ ■ ■	70	■ ■ ■ ■	7C	■ ■ ■ ■	73	■ ■ ■ ■	79	■ ■ ■ ■	64	■ ■ ■ ■
8D	■ ■ ■ ■	9E	■ ■ ■ ■	8F	■ ■ ■ ■	8F	■ ■ ■ ■	8E	■ ■ ■ ■	88	■ ■ ■ ■	8F	■ ■ ■ ■	91	■ ■ ■ ■	8E	■ ■ ■ ■
00	■ ■ ■ ■	10	■ ■ ■ ■	0C	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■
26	■ ■ ■ ■	30	■ ■ ■ ■	24	■ ■ ■ ■	2A	■ ■ ■ ■	36	■ ■ ■ ■	2E	■ ■ ■ ■	3E	■ ■ ■ ■	2F	■ ■ ■ ■	33	■ ■ ■ ■
42	■ ■ ■ ■	56	■ ■ ■ ■	44	■ ■ ■ ■	55	■ ■ ■ ■	59	■ ■ ■ ■	51	■ ■ ■ ■	51	■ ■ ■ ■	51	■ ■ ■ ■	54	■ ■ ■ ■
72	■ ■ ■ ■	78	■ ■ ■ ■	64	■ ■ ■ ■	71	■ ■ ■ ■	71	■ ■ ■ ■	71	■ ■ ■ ■	7E	■ ■ ■ ■	6F	■ ■ ■ ■	78	■ ■ ■ ■
8C	■ ■ ■ ■	96	■ ■ ■ ■	8E	■ ■ ■ ■	91	■ ■ ■ ■	91	■ ■ ■ ■	8E	■ ■ ■ ■	90	■ ■ ■ ■	81	■ ■ ■ ■	90	■ ■ ■ ■
00	■ ■ ■ ■	08	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■		
23	■ ■ ■ ■	3C	■ ■ ■ ■	32	■ ■ ■ ■	31	■ ■ ■ ■	31	■ ■ ■ ■	32	■ ■ ■ ■	31	■ ■ ■ ■	3E	■ ■ ■ ■		
44	■ ■ ■ ■	48	■ ■ ■ ■	52	■ ■ ■ ■	51	■ ■ ■ ■	55	■ ■ ■ ■	4C	■ ■ ■ ■	4A	■ ■ ■ ■	44	■ ■ ■ ■		
62	■ ■ ■ ■	6A	■ ■ ■ ■	72	■ ■ ■ ■	6A	■ ■ ■ ■	7B	■ ■ ■ ■	6C	■ ■ ■ ■	64	■ ■ ■ ■	68	■ ■ ■ ■		
8C	■ ■ ■ ■	84	■ ■ ■ ■	8D	■ ■ ■ ■	84	■ ■ ■ ■	91	■ ■ ■ ■	92	■ ■ ■ ■	98	■ ■ ■ ■	9E	■ ■ ■ ■		

DOT ON = 1  
DOT OFF = 0

### Numerals and Punctuation

HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE	
0E	■ ■ ■ ■	04	■ ■ ■ ■	1E	■ ■ ■ ■	1E	■ ■ ■ ■	06	■ ■ ■ ■	1F	■ ■ ■ ■	06	■ ■ ■ ■	1F	■ ■ ■ ■	0E	■ ■ ■ ■
33	■ ■ ■ ■	2C	■ ■ ■ ■	21	■ ■ ■ ■	21	■ ■ ■ ■	2A	■ ■ ■ ■	30	■ ■ ■ ■	28	■ ■ ■ ■	22	■ ■ ■ ■	31	■ ■ ■ ■
55	■ ■ ■ ■	44	■ ■ ■ ■	46	■ ■ ■ ■	4E	■ ■ ■ ■	5F	■ ■ ■ ■	5E	■ ■ ■ ■	5E	■ ■ ■ ■	44	■ ■ ■ ■	4E	■ ■ ■ ■
79	■ ■ ■ ■	64	■ ■ ■ ■	68	■ ■ ■ ■	61	■ ■ ■ ■	62	■ ■ ■ ■	61	■ ■ ■ ■	71	■ ■ ■ ■	68	■ ■ ■ ■	71	■ ■ ■ ■
8E	■ ■ ■ ■	8E	■ ■ ■ ■	9F	■ ■ ■ ■	9E	■ ■ ■ ■	82	■ ■ ■ ■	9E	■ ■ ■ ■	8E	■ ■ ■ ■	88	■ ■ ■ ■	8E	■ ■ ■ ■
0E	■ ■ ■ ■	0A	■ ■ ■ ■	0F	■ ■ ■ ■	06	■ ■ ■ ■	19	■ ■ ■ ■	08	■ ■ ■ ■	0C	■ ■ ■ ■	02	■ ■ ■ ■	08	■ ■ ■ ■
31	■ ■ ■ ■	3F	■ ■ ■ ■	34	■ ■ ■ ■	29	■ ■ ■ ■	3A	■ ■ ■ ■	34	■ ■ ■ ■	2C	■ ■ ■ ■	24	■ ■ ■ ■	24	■ ■ ■ ■
4F	■ ■ ■ ■	4A	■ ■ ■ ■	4E	■ ■ ■ ■	5C	■ ■ ■ ■	44	■ ■ ■ ■	4D	■ ■ ■ ■	44	■ ■ ■ ■	44	■ ■ ■ ■	44	■ ■ ■ ■
62	■ ■ ■ ■	7F	■ ■ ■ ■	65	■ ■ ■ ■	68	■ ■ ■ ■	6B	■ ■ ■ ■	72	■ ■ ■ ■	68	■ ■ ■ ■	64	■ ■ ■ ■	64	■ ■ ■ ■
8C	■ ■ ■ ■	8A	■ ■ ■ ■	9E	■ ■ ■ ■	9F	■ ■ ■ ■	93	■ ■ ■ ■	8D	■ ■ ■ ■	80	■ ■ ■ ■	82	■ ■ ■ ■	88	■ ■ ■ ■
0C	■ ■ ■ ■	04	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	00	■ ■ ■ ■	01	■ ■ ■ ■	04	■ ■ ■ ■	0A	■ ■ ■ ■	07	■ ■ ■ ■
2C	■ ■ ■ ■	24	■ ■ ■ ■	2C	■ ■ ■ ■	20	■ ■ ■ ■	20	■ ■ ■ ■	22	■ ■ ■ ■	24	■ ■ ■ ■	2A	■ ■ ■ ■	24	■ ■ ■ ■
48	■ ■ ■ ■	5F	■ ■ ■ ■	4C	■ ■ ■ ■	5F	■ ■ ■ ■	40	■ ■ ■ ■	44	■ ■ ■ ■	44	■ ■ ■ ■	40	■ ■ ■ ■	44	■ ■ ■ ■
64	■ ■ ■ ■	64	■ ■ ■ ■	64	■ ■ ■ ■	60	■ ■ ■ ■	6C	■ ■ ■ ■	68	■ ■ ■ ■	60	■ ■ ■ ■	60	■ ■ ■ ■	64	■ ■ ■ ■
80	■ ■ ■ ■	84	■ ■ ■ ■	88	■ ■ ■ ■	80	■ ■ ■ ■	8C	■ ■ ■ ■	90	■ ■ ■ ■	84	■ ■ ■ ■	80	■ ■ ■ ■	87	■ ■ ■ ■
10	■ ■ ■ ■	1C	■ ■ ■ ■	0E	■ ■ ■ ■	00	■ ■ ■ ■	0C	■ ■ ■ ■	0C	■ ■ ■ ■	02	■ ■ ■ ■	00	■ ■ ■ ■	08	■ ■ ■ ■
28	■ ■ ■ ■	24	■ ■ ■ ■	35	■ ■ ■ ■	20	■ ■ ■ ■	2C	■ ■ ■ ■	20	■ ■ ■ ■	24	■ ■ ■ ■	3F	■ ■ ■ ■	24	■ ■ ■ ■
44	■ ■ ■ ■	44	■ ■ ■ ■	57	■ ■ ■ ■	40	■ ■ ■ ■	40	■ ■ ■ ■	4C	■ ■ ■ ■	48	■ ■ ■ ■	40	■ ■ ■ ■	42	■ ■ ■ ■
62	■ ■ ■ ■	64	■ ■ ■ ■	70	■ ■ ■ ■	60	■ ■ ■ ■	6C	■ ■ ■ ■	64	■ ■ ■ ■	64	■ ■ ■ ■	7F	■ ■ ■ ■	64	■ ■ ■ ■
81	■ ■ ■ ■	9C	■ ■ ■ ■	8E	■ ■ ■ ■	9F	■ ■ ■ ■	8C	■ ■ ■ ■	88	■ ■ ■ ■	82	■ ■ ■ ■	80	■ ■ ■ ■	88	■ ■ ■ ■
0E	■ ■ ■ ■	06	■ ■ ■ ■	0C	■ ■ ■ ■	04	■ ■ ■ ■	11	■ ■ ■ ■	15	■ ■ ■ ■	04	■ ■ ■ ■	08	■ ■ ■ ■		
31	■ ■ ■ ■	24	■ ■ ■ ■	24	■ ■ ■ ■	24	■ ■ ■ ■	2A	■ ■ ■ ■	2E	■ ■ ■ ■	2A	■ ■ ■ ■	35	■ ■ ■ ■		
42	■ ■ ■ ■	48	■ ■ ■ ■	42	■ ■ ■ ■	40	■ ■ ■ ■	44	■ ■ ■ ■	5F	■ ■ ■ ■	51	■ ■ ■ ■	42	■ ■ ■ ■		
64	■ ■ ■ ■	64	■ ■ ■ ■	64	■ ■ ■ ■	64	■ ■ ■ ■	6E	■ ■ ■ ■	6E	■ ■ ■ ■	60	■ ■ ■ ■	60	■ ■ ■ ■		
88	■ ■ ■ ■	86	■ ■ ■ ■	8C	■ ■ ■ ■	84	■ ■ ■ ■	84	■ ■ ■ ■	95	■ ■ ■ ■	80	■ ■ ■ ■	80	■ ■ ■ ■		

DOT ON = 1  
DOT OFF = 0

\*CAUTION: No more than 128 LEDs "on" at one time at 100% brightness.

