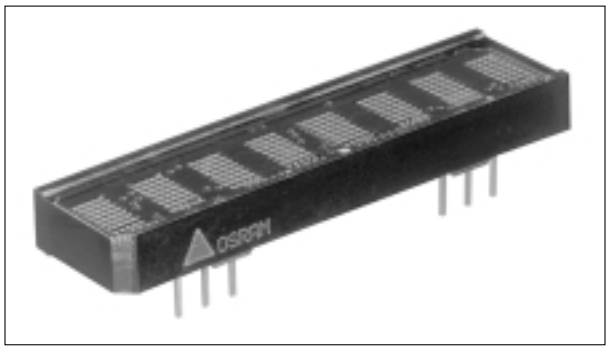
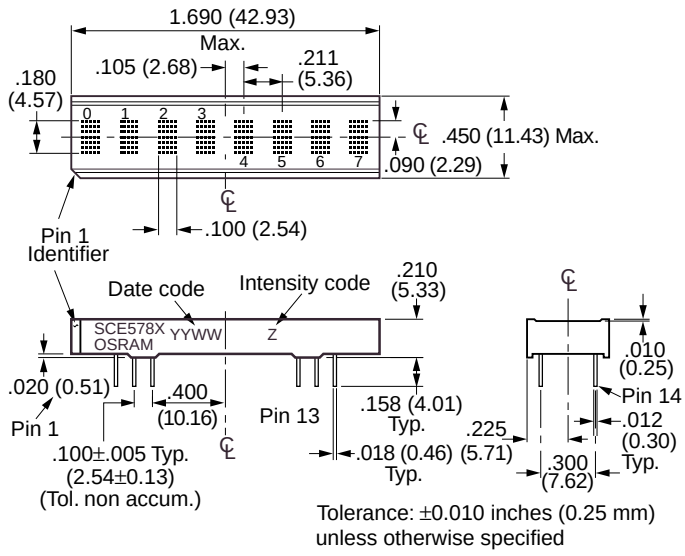
OSRAM

RED SCE5780
YELLOW SCE5781
HIGH EFFICIENCY RED SCE5782
GREEN SCE5783
HIGH EFFICIENCY GREEN SCE5784
SOFT ORANGE SCE5785
(Preliminary) InGaAlP RED SCE5786

0.180" 8-Character 5 x 7 Dot Matrix
Serial Input Dot Addressable Intelligent Display® Devices



Dimensions in Inches (mm)



FEATURES

- **Eight 0.180" (4.57 mm) 5 x 7 Dot Matrix Characters in Red, Yellow, High Efficiency Red, Green, High Efficiency Green, Soft Orange, or InGaAlP Red**
- **ROMless Serial Input, Dot Addressable Display Ideal for User Defined Characters**
- **Built-in Decoders, Multiplexers and LED Drivers**
- **Readable from 8 Feet (2.5 meters)**
- **Programmable Features:**
  - **Clear Function**
  - **Eight Dimming Levels**
  - **Peak Current Select**
  - **(12.5% or Full Peak Current)**
  - **Prescaler Function (External Oscillator Divided by 16 or 1)**
  - **Internal or External Clock**

DESCRIPTION

The SCE5780 (red), SCE5781 (yellow), SCE5782 (HER), SCE5783 (green), SCE5784 (HEG), SCE5785 (orange), and SCE5786 (InGaAlP red) are eight digit, dot addressable 5x7 dot matrix, serial input, Intelligent Display devices. The eight 0.180" (4.57 mm) high digits are packaged in a rugged, high quality, optically transparent, plastic 26 pin DIP with 0.3" pin spacing.

The on-board CMOS has a 280 bit RAM, one bit associated with one LED, each to generate User Defined Characters.

The SCE578X is designed to work with the serial port of most common microprocessors. Data is transferred into the display through the Serial Data Input (DATA), clocked by the Serial Data Clock (SDCLK), and enabled by the Load Input (LOAD).

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DESCRIPTION (continued)

The Clock I/O (CLK I/O) and Clock Select ($\overline{\text{CLKSEL}}$) pins offer the user the capability to supply a high speed external multiplex clock. This feature can minimize audio in-band interference for portable communication equipment or eliminate the visual synchronization effects found in high vibration environments such as avionic equipment. The prescaler function allows for a higher speed external multiplex clock when set to divide by 16.

Maximum Ratings

V_{CC}, Logic Supply Voltage (non-operating) ..... –0.5 to +7.0 Vdc
V_{LL}, LED Supply Voltage (non-operating)..... –0.5 to 5.5 Vdc
Input Voltage Levels Relative
to Ground..... –0.5 to V_{CC} +0.5 Vdc
Operating Temperature [1] ..... –40°C to +85°C
Storage Temperature..... –40°C to +100°C
Maximum Solder Temperature 0.063"
below Seating Plane, t<5 s.....260°C
Relative Humidity at 85°C 85%
Maximum Power Dissipation
70°C.....1.7 W
85°C.....1.25 W
ESD (100 pF, 1.5 kΩ) ..... 2.0 kV
Maximum Input Current.....±100 mA

Note:

1) For operation at high temperature, see Thermal Considerations.

Switching Specifications

(over operating temperature range and V_{CC}=4.5 V to 5.5 V)

Symbol	Description	Min.	Units
T_{RC}	Reset Active Time	600	ns
T_{LDS}	Load Setup Time	50	ns
T_{DS}	Data Setup Time	50	ns
T_{SDCLK}	Clock Period	200	ns
T_{SDCW}	Clock Width	70	ns
T_{LDH}	Load Hold Time	0	ns
T_{DH}	Data Hold Time	25	ns
T_{WR}	Total Write Time	2.2	µs
T_{BL}	Time Between Loads	600	ns

Note:

T_{SDCW} is the minimum time the SDCLK may be low or high. The SDCLK period must be a minimum of 200 ns.

Figure 1. Timing Diagram—Data Write Cycle

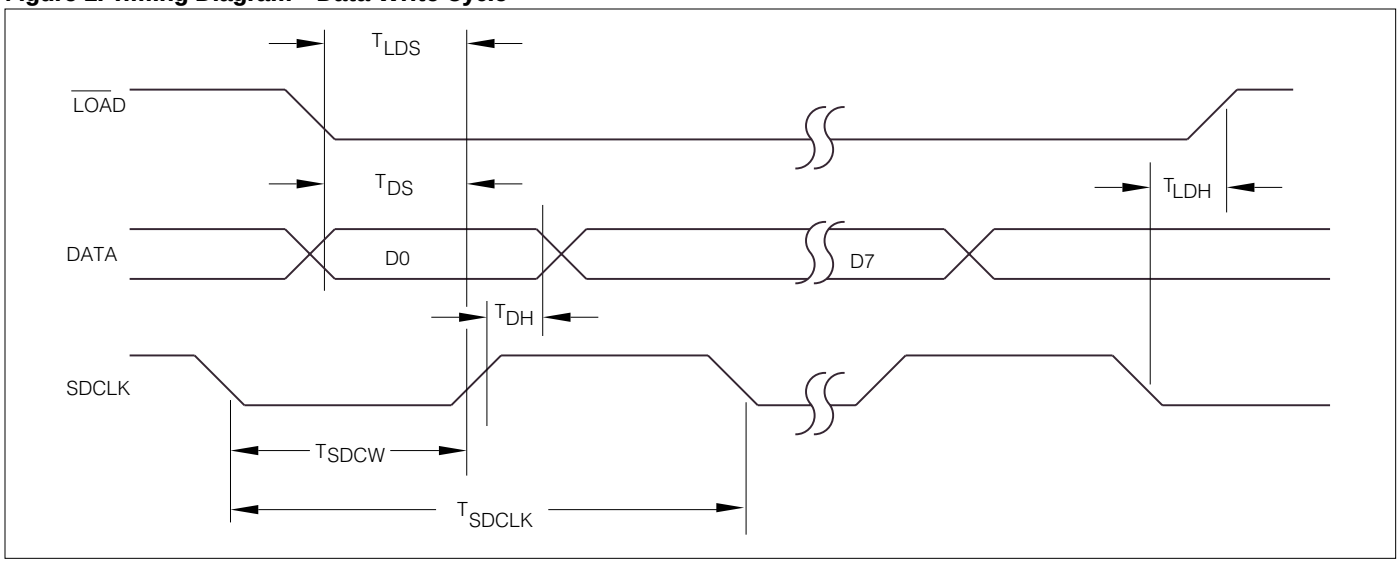
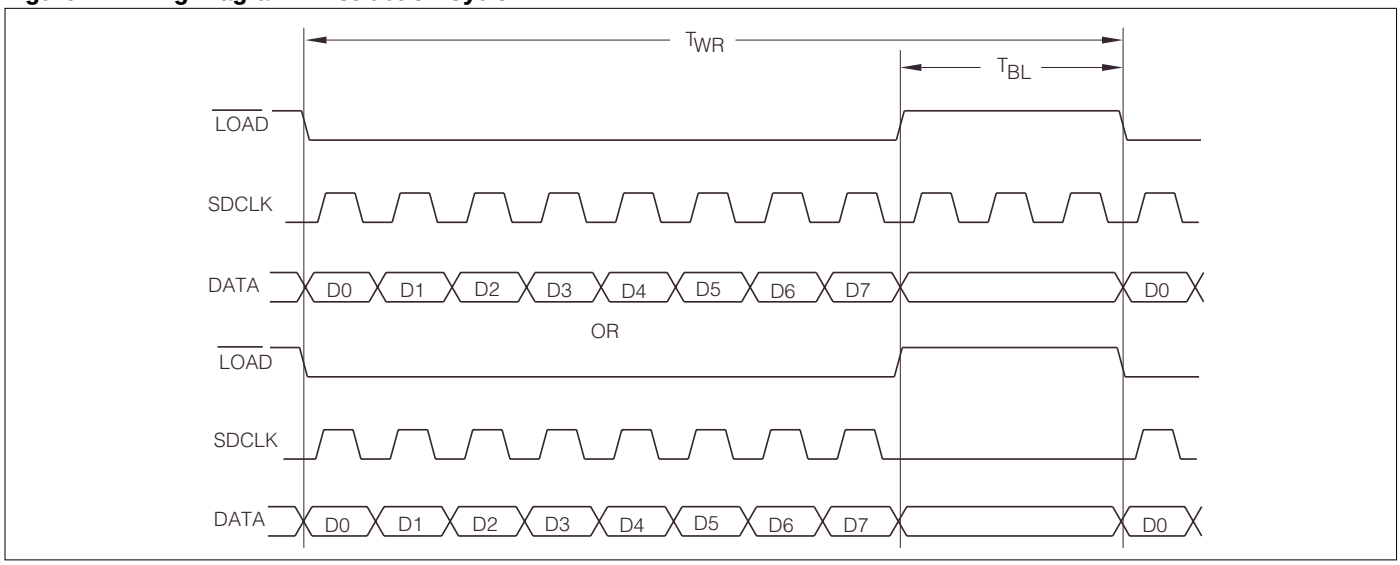


Figure 2. Timing Diagram—Instruction Cycle



Electrical Characteristics (over operating temperature)

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{CC}	4.5	5.0	5.5	V	—
V_{LL}	3.0	—	5.5	V	—
I_{CC} (PWR DWN)(4)	—	—	100	µA	V_{CC}=V_{LL}=5.0 V, all inputs=0 V or V_{CC}
I_{LL} (PWR DWN)(4)	—	—	50	µA	—
I_{CC}	—	—	2.0	mA	V_{CC}=5.0 V
I_{LL} (20 dots/char)(1)(2)	—	240	345	mA	V_{CC}=V_{LL}=5.0 V, "#" displayed in 8 digits, brightness=100%, I_P=100% at 25°C
I_{IL}	—	—	–10	µA	V_{CC}=5.0 V, all inputs=0 V
I_{IH}	—	—	10	µA	V_{CC}=V_{IN}=5.0 V (all inputs)
V_{IH}	3.5	—	—	V	V_{CC}=4.5 V to 5.5 V
V_{IL}	—	—	1.5	V	V_{CC}=4.5 V to 5.5 V
I_{OH} (CLK I/O)	—	–8.9	—	mA	V_{CC}=4.5 V, V_{OH}=2.4 V
I_{OL} (CLK I/O)	—	1.6	—	mA	V_{CC}=4.5 V, V_{OH}=0.4 V
$\theta_{JC\text{-}pin}$	—	34	—	°C/W	—
Internal OSC Frequency	120	—	347	kHz	V_{CC}=5.0 V, $\overline{\text{CLKSEL}}$=1, Prescale=÷1
External OSC Frequency	120	—	347	kHz	V_{CC}=5.0 V, $\overline{\text{CLKSEL}}$=0, Prescale=÷1
External OSC Frequency with Prescale	1.92	—	5.55	MHz	V_{CC}=5.0 V, $\overline{\text{CLKSEL}}$=0, Prescale=÷16
Mux Frequency(3)	375	768	1086	Hz	—

Notes:

1) Peak current=1.87 x I_{LL} x I_{LL} varies with V_{LL} Normalized curve, Figure 12.
2) Unused inputs must be tied high.
3) Mux rate=[OSC Frequency/(64 x 7)].
4) External oscillator must be stopped during power down mode for minimum current.

Input/Output Circuits

Figures 3 and 4 show the input and output resistor/diode networks used for ESD protection and to eliminate substrate latch-up caused by input voltage over/under shoot.

Figure 3. Inputs

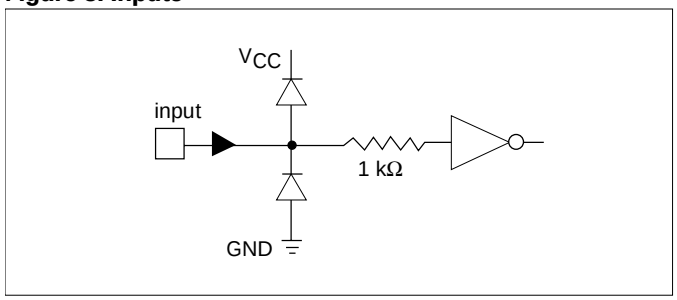
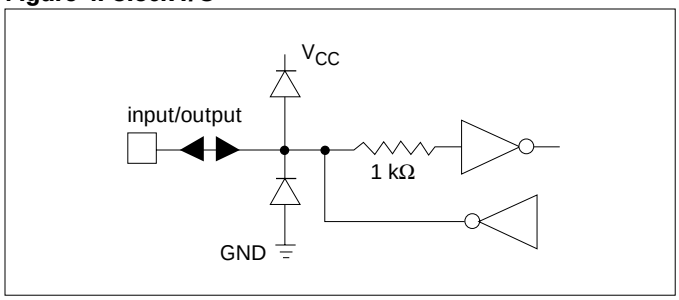


Figure 4. Clock I/O



Optical Characteristics at 25°C

(V_{LL}=V_{CC}=5.0 V at 100% brightness level, viewing angle: X axis ±55°, Y axis ±65°)

Red SCE5780

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	37.5	90.0	µcd/dot
Peak Wavelength	λ_{peak}	—	660	nm
Dominant Wavelength	λ_{dom}	—	639	nm

Yellow SCE5781

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	75	110	µcd/dot
Peak Wavelength	λ_{peak}	—	585	nm
Dominant Wavelength	λ_{dom}	—	583	nm

High Efficiency Red SCE5782

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	75	190	µcd/dot
Peak Wavelength	λ_{peak}	—	630	nm
Dominant Wavelength	λ_{dom}	—	626	nm

Green SCE5783

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	75	150	µcd/dot
Peak Wavelength	λ_{peak}	—	565	nm
Dominant Wavelength	λ_{dom}	—	570	nm

High Efficiency Green SCE5784

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	120	215	µcd/dot
Peak Wavelength	λ_{peak}	—	568	nm
Dominant Wavelength	λ_{dom}	—	574	nm

Soft Orange SCE5785

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	120	150	µcd/dot
Peak Wavelength	λ_{peak}	—	610	nm
Dominant Wavelength	λ_{dom}	—	605	nm

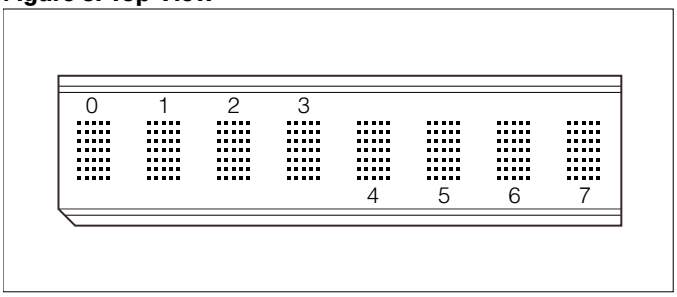
InGaAlP Red SCE5786 (Preliminary)

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	375	950	µcd/dot
Peak Wavelength	λ_{peak}	—	642	nm
Dominant Wavelength	λ_{dom}	—	630	nm

Notes:

1. Dot to dot intensity matching at 100% brightness is 1.8:1.
2. Display are binned for hue at 2.0 nm intervals for yellow, green, and high efficiency green.
3. Displays within a given intensity category have an intensity matching of 1.5:1 (max.)

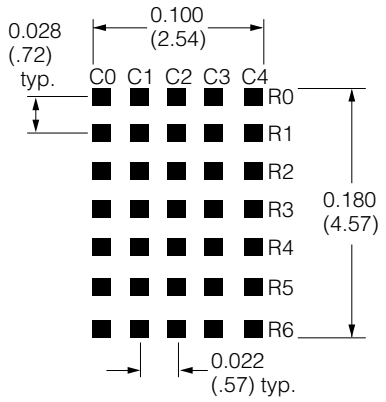
Figure 5. Top View



Pin Assignment

Pin	Function	Pin	Function
1	$\overline{\text{CLKSEL}}$	14	Serial Data
2	V_{CC} (Logic)	15	No connect
3	V_{LL} (LED)	16	Serial CLK
4	No pin	17	No pin
5	No pin	18	No pin
6	No pin	19	No pin
7	No pin	20	No pin
8	No pin	21	No pin
9	No pin	22	No pin
10	No pin	23	No pin
11	Load	24	Reset
12	GND	25	CLK I/O
13	GND	26	No connect

Figure 6. Dot Matrix Format



Pin Definitions

Pin	Function	Definitions
1	$\overline{\text{CLKSEL}}$	H=internal clock, L=external clock
2	V_{CC} (Logic)	Logic power supply
3	V_{LL} (LED)	LED power supply
4–10	No pin	No pins in these positions
11	Load	Low input enables data clocking into the 8-bit serial shift register. When Load goes high, the contents of the 8-bit serial shift register will be decoded.
12,13	GND	Power supply ground
14	Serial Data	Serial data input
15	No connect	Pin has no function
16	Serial CLK	For loading data into the 8-bit serial register on a low to high transition
17–23	No pin	No pins in these positions
24	Reset	Asynchronous input, when low will clear the Multiplex Counter, User RAM, and Data Register. Control Word Register is set to 100% brightness, maximum peak current, and oscillator divided by 1. The display blanked.
25	CLK I/O	Outputs master clock or input external clock for display multiplexing.
26	No connect	Pin has no function

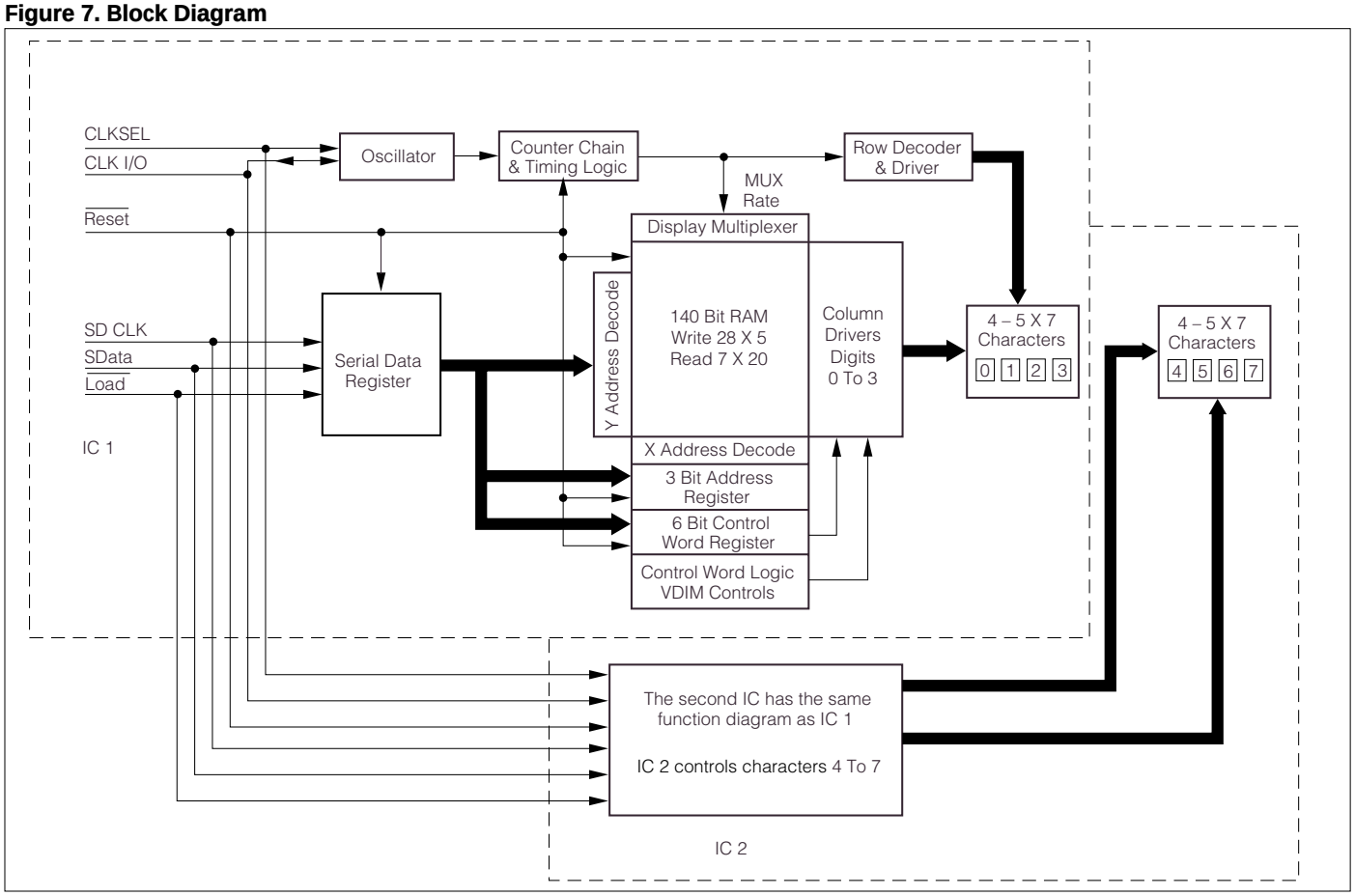
Display Column and Row Format

	C0	C1	C2	C3	C4
Row 0	1	1	1	1	1
Row 1	0	0	1	0	0
Row 2	0	0	1	0	0
Row 3	0	0	1	0	0
Row 4	0	0	1	0	0
Row 5	0	0	1	0	0
Row 6	0	0	1	0	0
1=Display dot “On” 0=Display dot “Off”					

Column Data Ranges

Row 0	00H to 1FH
Row 1	00H to 1FH
Row 2	00H to 1FH
Row 3	00H to 1FH
Row 4	00H to 1FH
Row 5	00H to 1FH
Row 6	00H to 1FH

Figure 7. Block Diagram



Operation of the SCE578X

The SCE578X display consists of two CMOS ICs containing control logic and drivers for eight 5 x 7 characters. The first IC controls characters 0 through 3 and the second IC controls characters 4 through 7. These components are assembled in a compact plastic package.

Individual LED dot addressability allows the user great freedom in creating special characters or mini-icons.

The serial data interface provides a highly efficient interconnection between the display and the mother board. The SCE578X requires a minimum three input lines as compared to fourteen for an equivalent eight character parallel input part.

The on-board CMOS IC is the electronic heart of the display. Each IC accepts serially formatted data, which is stored in the internal RAM. The IC accepts data based on the character address selected. The first IC is selected when addressing characters 0 through 3, the second IC is selected when addressing characters 4 though 7, and both ICs are selected when the Control Word is addressed.

Asynchronously the RAM is read by the character multiplexer at a strobe rate that results in a flicker free display. Figure 7 shows the three functional areas of the IC. These include: the input serial data register and control logic, a 140 bit two port RAM, and an internal multiplexer/display driver. The second IC is identical except characters 4 though 7 are driven.

The following explains how to format the serial data to be loaded into the display. The user supplies a string of bit mapped decoded characters. The contents of this string is shown in Figure 8a. Figure 8b shows that each character consist of eight 8 bit words. The first word encodes the display

character location and the succeeding seven bytes are row data. The row data represents the status (On, Off) of individual column LEDs. Figure 8c shows that each 8 bit word is formatted to represent Character Address, or Column Data.

Figure 8d shows the sequence for loading the bytes of data. Bringing the $\overline{\text{LOAD}}$ line low enables the serial register to accept data. The shift action occurs on the low to high transition of the serial data clock (SDCLK). The least significant bit (D0) is loaded first. After eight clock pulses the $\overline{\text{LOAD}}$ line is brought high. With this transition the OPCODE is decoded. The decoded OPCODE directs D4–D0 to be latched in the Character Address register, stored in the RAM as Column data, or latched in the Control Word register. The control IC requires a minimum 600 ns delay between successive byte loads. As indicated in Figure 8a, a total of 512 bits of data are required to load all eight characters into the display.

The Character Address Register selects the character address that the row and column data will be written to. See Table 2 for opcode and character addressing. After loading the Character Address Register, the next seven bytes load the column data, one row at a time, starting with row 0 (top row) and ending with row 6 (bottom row). Each character address has a 7 x 5 bit User RAM formatted as seven rows, each containing five column data bits. The three most significant bits, D7–D5 represent the opcode for the row data and the least significant five bits, D4–D0 represent the column data. See Table 3 for the column data format. If an address is loaded before all seven rows are written, the next column data will be loaded into Row 0 of the new address. The remaining rows of the old address are not changed.

Table 1 shows the Row Address for the example character, "D." Column data is written and read asynchronously from the 280 bit RAM. Once loaded, the internal oscillator and character multiplexer reads the data from the RAM. These characters are row strobed with column data as shown in Figures 9 and 10. The character strobe rate is determined by the internal or user supplied external MUX Clock and the ICs÷ 320 counter.

Table 1. Character "D"

	Op code			Column Data					Hex
	D7	D6	D5	D4 C0	D3 C1	D2 C2	D1 C3	D0 C4	
Row 0	0	0	0	1	1	1	1	0	1E
Row 1	0	0	0	1	0	0	0	1	11
Row 2	0	0	0	1	0	0	0	1	11
Row 3	0	0	0	1	0	0	0	1	11
Row 4	0	0	0	1	0	0	0	1	11
Row 5	0	0	0	1	0	0	0	1	11
Row 6	0	0	0	1	1	1	1	0	1E

Figure 8. Loading Serial Character Data

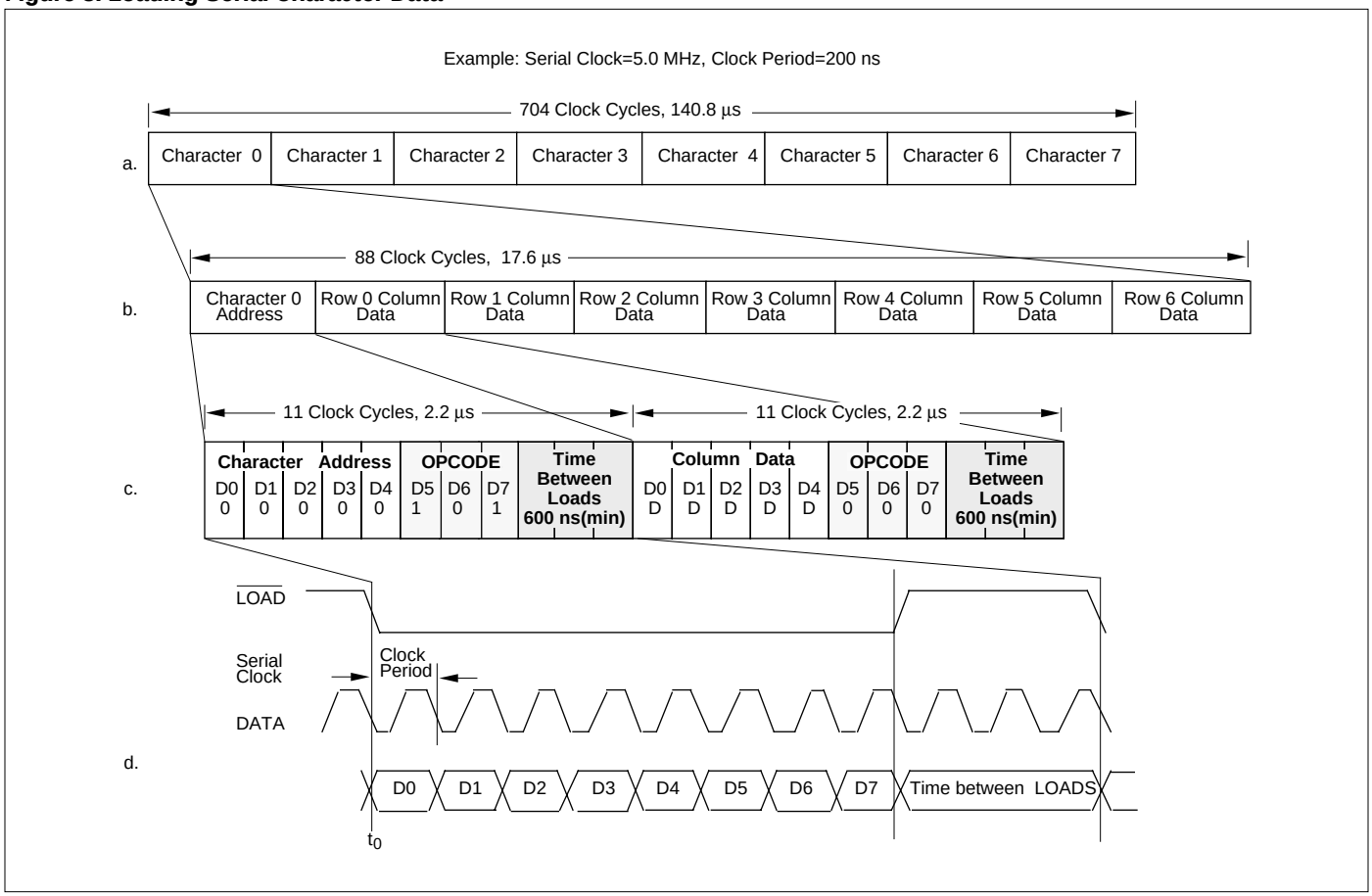


Table 2. Load Character Address

Op code D7	D6	D5	Character Address D4	D3	D2	D1	D0	Hex	Operation Load
1	0	1	0	0	0	0	0	A0	Character 0
1	0	1	0	0	0	0	1	A1	Character 1
1	0	1	0	0	0	1	0	A2	Character 2
1	0	1	0	0	0	1	1	A3	Character 3
1	0	1	0	0	1	0	0	A4	Character 4
1	0	1	0	0	1	0	1	A5	Character 5
1	0	1	0	0	1	1	0	A6	Character 6
1	0	1	0	0	1	1	1	A7	Character 7

Table 3. Load Column Data

Op code D7	D6	D5	Column Data D4	D3	D2	D1	D0	Operation Load
0	0	0	C0	C1	C2	C3	C4	Row 0
0	0	0	C0	C1	C2	C3	C4	Row 1
0	0	0	C0	C1	C2	C3	C4	Row 2
0	0	0	C0	C1	C2	C3	C4	Row 3
0	0	0	C0	C1	C2	C3	C4	Row 4
0	0	0	C0	C1	C2	C3	C4	Row 5
0	0	0	C0	C1	C2	C3	C4	Row 6

The user can activate four Control functions. These include: LED Brightness Level, IC Power Down, Prescaler, or Display Clear. OPCODEs and six bit words are used to initiate these functions. The OPCODEs and Control Words for the Character Address and Loading Column Data are shown in Tables 2 and 3.

The user can select eight specific LED brightness levels, Tables 4 and 5. Depending on how D3 is selected either one (1) for maximum peak current or zero (0) for 12.5% of maximum peak current in the control word per Table 4 and 5, the user can select 16 specific LED brightness levels. These brightness levels (in percentages of full brightness of the display) depending on how the user selects D3 can be one (1) or zero (0) are as follows: 100% ($E0_{HEX}$ or $E8_{HEX}$), 53% ($E1_{HEX}$ or $E9_{HEX}$), 40% ($E2_{HEX}$ or EA_{HEX}), 27% ($E3_{HEX}$ or EB_{HEX}), 20% ($E4_{HEX}$ or EC_{HEX}), 13% ($E5_{HEX}$ or ED_{HEX}), and 6.6% ($E6_{HEX}$ or EE_{HEX}), 0.0% ($E7_{HEX}$ or EF_{HEX}). The brightness levels are controlled by changing the duty factor of the row strobe pulse.

The SCE578X offers a unique Display Power Down feature which reduces I_{CC} to less than 150 µA total. When EF_{HEX} is loaded (Table 6) the display is set to 0% brightness. When in the Power Down mode data may still be written into the RAM. The display is reactivated by loading a new brightness Level Control Word into the display.

Table 4. Display Brightness

Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	0	0	0	0	0	E0	100%
1	1	1	0	0	0	0	1	E1	53%
1	1	1	0	0	0	1	0	E2	40%
1	1	1	0	0	0	1	1	E3	27%
1	1	1	0	0	1	0	0	E4	20%
1	1	1	0	0	1	0	1	E5	13%
1	1	1	0	0	1	1	0	E6	6.6%
1	1	1	0	0	1	1	1	E7	0.0%

Table 5. Display Brightness

Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	0	1	0	0	0	E8	100%
1	1	1	0	1	0	0	1	E9	53%
1	1	1	0	1	0	1	0	EA	40%
1	1	1	0	1	0	1	1	EB	27%
1	1	1	0	1	1	0	0	EC	20%
1	1	1	0	1	1	0	1	ED	13%
1	1	1	0	1	1	1	0	EE	6.6%
1	1	1	0	1	1	1	1	EF	0.0%

Table 6. Power Down

Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	0	1	1	1	1	EF	0% brightness

Figure 9. Row and Column Locations for a Character "D"

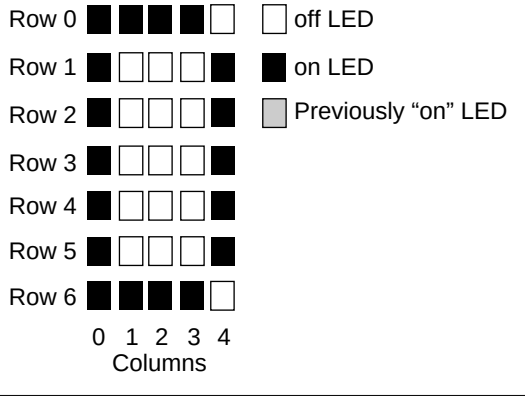
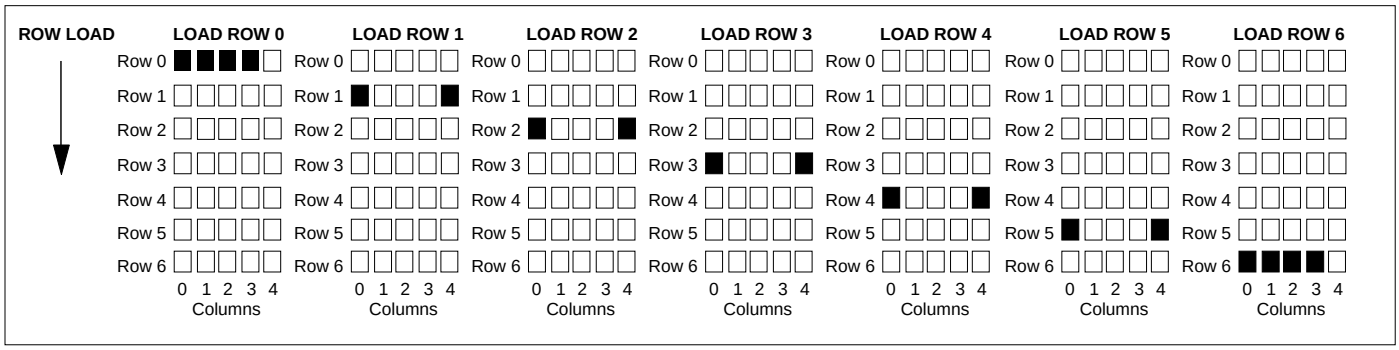


Figure 10. Row Strobing



The SCE578X allows a high frequency external oscillator source to drive the display. Data bit, D4, in the control word format controls the prescaler function. The prescaler allows the oscillator source to be divided by 16 by setting D4=1. However, the prescaler should not be used, i.e., when using the internal oscillator source.

The Software Clear ($C0_{HEX}$), given in Table 7, clears the Address Register and the RAM. The display is blanked and the Character Address Register will be set to Character 0. The internal counter and the Control Word Register are unaffected. The Software Clear will remain active until the next data input cycle is initiated.

Table 7. Software Clear

Op code D7	D6	Control Word D5	D4	D3	D2	D1	D0	Hex	Operation
1	1	0	0	0	0	0	0	C0	CLEAR

Multiplexer and Display Driver

The eight characters are row multiplexed with RAM resident column data. The strobe rate is established by the internal or external MUX Clock rate. The MUX Clock frequency is divided by a 320 counter chain. This results in a typical strobe rate of 768 Hz. By pulling the Clock SEL line low, the display can be operated from an external MUX Clock. The external clock is attached to the CLK I/O connection.

An asynchronous hardware Reset (pin 24) is also provided. Bringing this pin low will clear the Character Address Register, Control Word Register, RAM, and blanks the display. This action leaves the display set at Character Address 0, and the Brightness Level set at 100%, prescaler ÷1.

Electrical and Mechanical Considerations

Thermal Considerations

The display's power usage may need to be reduced to operate at high ambient temperatures. The power may be reduced by lowering the brightness level, reducing the total number of LEDs illuminated, or lowering V_{LED}. The V_{CC} supply, relative to the V_{LED} supply, has little effect on the power dissipation of the display and is not considered when determining the power dissipation.

To determine the power deration with a given ambient temperature, use the following formula:

$$T_{jmax} = T_A + P_D \cdot \theta_{ja}$$

where: T_{jmax}=maximum IC junction temperature
P_D=power dissipated by the ICs
θ_{ja}=thermal resistance, junction to ambient

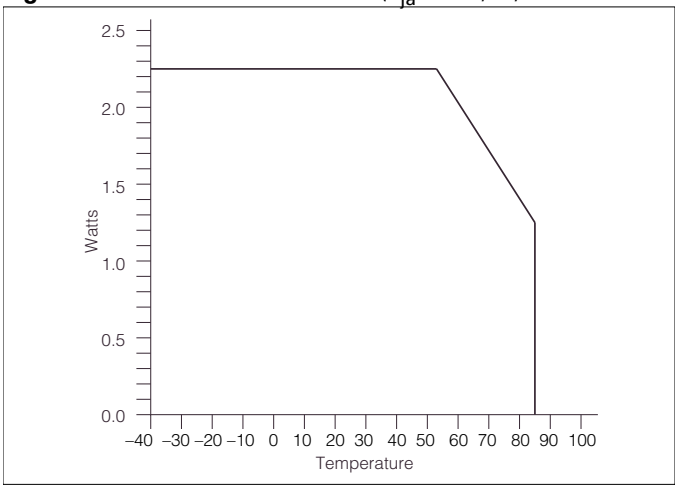
To determine the power dissipation of the display, use the following formula:

$$PD = N \cdot I_{LL} / 140 \cdot RB$$

where: N=number of LEDs on
I_{LL}/140=average current for a single LED
RB=relative brightness level

A typical thermal resistance value (q_{ja}) for this display is 50°C/W when mounted in a socket soldered on a 0.062" thick PCB with 0.020", 1 ounce copper traces and the display covered by a plastic filter. The display's maximum IC junction temperature is 125°C. Power Deration Curve is based on these typical values.

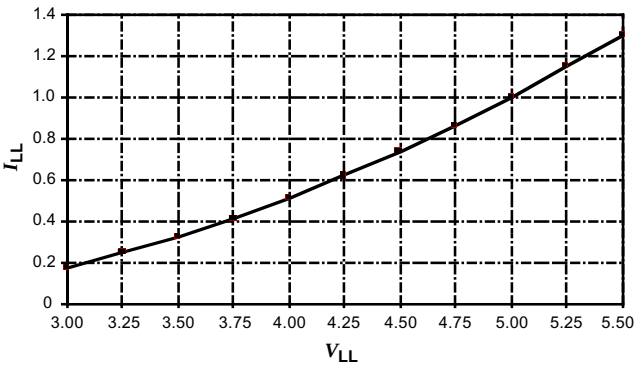
Figure 11. Power Deration Curve (θ_{ja}=50°C/W)



V_{CC} and V_{LL} are two separate power supplies sharing a common ground. V_{CC} supplies power for all the display logic. V_{LL} supplies the power for the LEDs. By separating the two supplies, V_{CC} and V_{LL} can be varied independently and keeps the logic supply clean.

V_{LL} can be varied between 3.0 volts and 5.5 volts. The LED drive current will vary with changes in V_{LL}. See Figure 12 for I_{LL} variance.

Figure 12. I_{LL} Variance



V_{CC} can vary between 4.5 volts and 5.5 volts. Operation below 4.5 volts will change the timing and switching levels of the inputs.

Interconnect Considerations

Optimum product performance can be had when the following electrical and mechanical recommendations are adopted. The SCE578X's IC is constructed in a high speed CMOS process; consequently high speed noise on the SERIAL DATA, SERIAL DATA CLOCK, $\overline{\text{LOAD}}$ and $\overline{\text{RESET}}$ lines may cause incorrect data to be written into the serial shift register. Adhere to transmission line termination procedures when using fast line drivers and long cables (>10 cm).

Good ground and power supply decoupling will insure that I_{CC} (<800 mA peak) switching currents do not generate localized ground bounce. Therefore it is recommended that each display package use a 0.1 µF and 20 µF tantulum capacitor between V_{CC} and ground.

When the internal MUX Clock is being used connect the $\overline{\text{CLKSEL}}$ pin to V_{CC}. In those applications where $\overline{\text{RESET}}$ will not be connected to the system's reset control, it is recommended that this pin be connected to the center node of a series 0.1 µF and 100 kΩ RC network. Thus upon initial power up the $\overline{\text{RESET}}$ will be held low for 10 ms allowing adequate time for the system power supply to stabilize.

ESD Protection

The input protection structure of the SCE578X provides significant protection against ESD damage. It is capable of withstanding discharges greater than 2.0 kV. Take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in antistatic packaging.

Soldering Considerations

The SCE578X can be hand soldered with SN63 solder using a grounded iron set to 260°C.

Wave soldering is also possible following these conditions: Preheat that does not exceed 93°C on the solder side of the PC board or a package surface temperature of 85°C. Water soluble organic acid flux (except carboxylic acid) or resin-based RMA flux without alcohol can be used.

Wave temperature of 245°C ±5°C with a dwell between 1.5 sec. to 3.0 sec. Exposure to the wave should not exceed temperatures above 260°C for five seconds at 0.063" below the seating plane. The packages should not be immersed in the wave.

Post Solder Cleaning Procedures

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the nylon package. For further information refer to Appnotes 18 and 19.

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 14 pin DIP sockets .300" wide with .100" centers work well for single displays. Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtown, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardward, New Albany, IN.

For further information refer to Appnote 22.

Optical Considerations

The 0.180" high character of the SCE578X gives readability up to five feet. Proper filter selection enhances readability over this distance.

Using filters emphasizes the contrast ratio between a lit LED and the character background. This will increase the discrimination of different characters. The only limitation is cost. Take into consideration the ambient lighting environment for the best cost/benefit ratio for filters.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are an inexpensive and effective way to strengthen contrast ratios. The SCE5780 is a red display and should be used with long wavelength pass filter having a sharp cut-off in the 600 nm to 620 nm range. The SCE5782 is a high efficiency red display and should be used with long wavelength pass filter having a sharp cut-off in the 570 nm to 600 nm range. The SCE5784 is a high efficiency green display and should be used with long wavelength pass filter that peaks at 565 nm. The SCE5785 is a soft orange display and should be used with long wavelength pass filter that peaks at 610 nm. The SCE5786 is an InGaAlP red display and should be used with long wavelength pass filter that peaks at 645 nm.

Additional contrast enhancement is gained by shading the displays. Plastic band-pass filters with built-in louvers offer the next step up in contrast improvement. Plastic filters can be improved further with anti-reflective coatings to reduce glare. The trade-off is fuzzy characters. Mounting the filters close to the display reduces this effect. Take care not to overheat the plastic filter by allowing for proper air flow.

Optimal filter enhancements are gained by using circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1.0%.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homalite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY, Hoya Optics, Inc., Fremont, CA.

One last note on mounting filters: recessing displays and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several Bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.-Atlas, Van Nuys, CA.

Microprocessor Interface

The microprocessor interface is through the serial port, SPI port or one out of eight data bits on the eight bit parallel port and also control lines $\overline{\text{SDCLK}}$ and $\overline{\text{LOAD}}$.

Power Up Sequence

Upon power up display will come on at random. Thus the display should be reset at power-up. The reset will set the Address Register to Digit 0, User RAM is set to 0 (display blank) the Control Word is set to 0 (100% brightness) and the internal counters are reset.

Loading Data into the Display

Use following procedure to load data into the display:

1. Power up the display.
2. Bring $\overline{\text{RST}}$ low (600 ns duration minimum) to clear the Multiplex Counter, Address Register, Control Word Register, User Ram and Data Register. The display will be blank. Display brightness is set to 100%.
3. If a different brightness is desired, load the proper brightness opcode into the Control Word Register.
4. Load the Digit Address into the display.
5. Load display row and column data for the selected digit.
6. Repeat steps 4 and 5 for all digits.

Data Contents for the Word "ABCDEFGH"

Step	D7	D6	D5	D4	D3	D2	D1	D0	Function
A	1	1	0	0	0	0	0	0	CLEAR
B	1	1	1	0	0	0	0	0	100% BRIGHTNESS
1	1	0	1	0	0	0	0	0	DIGIT D0 SELECT
2	0	0	0	0	0	1	0	0	ROW 0 (A)
3	0	0	0	0	1	0	1	0	ROW 1 (A)
4	0	0	0	1	0	0	0	1	ROW 2 (A)
5	0	0	0	1	1	1	1	1	ROW 3 (A)
6	0	0	0	1	0	0	0	1	ROW 4 (A)
7	0	0	0	1	0	0	0	1	ROW 5 (A)
8	0	0	0	1	0	0	0	1	ROW 6 (A)
9	1	0	1	0	0	0	0	1	DIGIT D1 SELECT
10	0	0	0	1	1	1	1	1	ROW 0 (B)
11	0	0	0	1	0	0	0	1	ROW 1 (B)
12	0	0	0	1	0	0	0	1	ROW 2 (B)
13	0	0	0	1	1	1	1	0	ROW 3 (B)
14	0	0	0	1	0	0	0	1	ROW 4 (B)
15	0	0	0	1	0	0	0	1	ROW 5 (B)
16	0	0	0	1	1	1	1	1	ROW 6 (B)
17	1	0	1	0	0	0	1	0	DIGIT D2 SELECT
18	0	0	0	0	0	1	1	1	ROW 0 (C)
19	0	0	0	0	1	0	0	0	ROW 1 (C)
20	0	0	0	1	0	0	0	0	ROW 2 (C)
21	0	0	0	1	0	0	0	0	ROW 3 (C)
22	0	0	0	1	0	0	0	0	ROW 4 (C)
23	0	0	0	0	1	0	0	0	ROW 5 (C)
24	0	0	0	0	0	1	1	1	ROW 6 (C)
25	1	0	1	0	0	0	1	1	DIGIT D3 SELECT
26	0	0	0	1	1	1	1	0	ROW 0 (D)
27	0	0	0	1	0	0	0	1	ROW 1 (D)
28	0	0	0	1	0	0	0	1	ROW 2 (D)
29	0	0	0	1	0	0	0	1	ROW 3 (D)
30	0	0	0	1	0	0	0	1	ROW 4 (D)
31	0	0	0	1	0	0	0	1	ROW 5 (D)
32	0	0	0	1	1	1	1	0	ROW 6 (D)
33	1	0	1	0	0	1	0	0	DIGIT D4 SELECT
34	0	0	0	1	1	1	1	1	ROW 0 (E)
35	0	0	0	1	0	0	0	0	ROW 1 (E)
36	0	0	0	1	0	0	0	0	ROW 2 (E)
37	0	0	0	1	1	1	1	0	ROW 3 (E)
38	0	0	0	1	0	0	0	0	ROW 4 (E)
39	0	0	0	1	0	0	0	0	ROW 5 (E)
40	0	0	0	1	1	1	1	1	ROW 6 (E)
41	1	0	1	0	0	1	0	1	DIGIT D5 SELECT
42	0	0	0	1	1	1	1	1	ROW 0 (F)
43	0	0	0	1	0	0	0	0	ROW 1 (F)
44	0	0	0	1	0	0	0	0	ROW 2 (F)
45	0	0	0	1	1	1	1	0	ROW 3 (F)
46	0	0	0	1	0	0	0	0	ROW 4 (F)
47	0	0	0	1	0	0	0	0	ROW 5 (F)
48	0	0	0	1	0	0	0	0	ROW 6 (F)
49	1	0	1	0	0	1	1	0	DIGIT D6 SELECT
50	0	0	0	0	1	1	1	0	ROW 0 (G)
51	0	0	0	1	0	0	0	1	ROW 1 (G)
52	0	0	0	1	0	0	0	0	ROW 2 (G)
53	0	0	0	1	0	0	0	0	ROW 3 (G)
54	0	0	0	1	0	0	1	1	ROW 4 (G)
55	0	0	0	1	0	0	0	1	ROW 5 (G)
56	0	0	0	0	1	1	1	0	ROW 6 (G)
57	1	0	1	0	0	1	1	1	DIGIT D7 SELECT
58	0	0	0	1	0	0	0	1	ROW 0 (H)
59	0	0	0	1	0	0	0	1	ROW 1 (H)
60	0	0	0	1	0	0	0	1	ROW 2 (H)
61	0	0	0	1	1	1	1	1	ROW 3 (H)
61	0	0	0	1	0	0	0	1	ROW 4 (H)
62	0	0	0	1	0	0	0	1	ROW 5 (H)
63	0	0	0	1	0	0	0	1	ROW 6 (H)

Figure 13. Display Interface to Siemens/Intel 8031 Microprocessor (using serial port in mode 0)

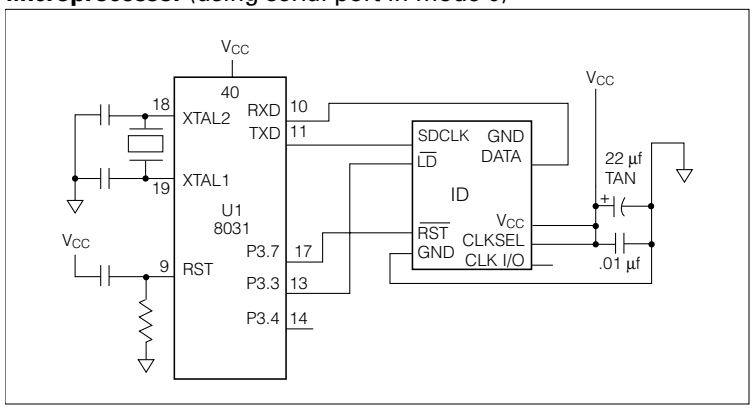


Figure 14. Display Interface to Siemens/Intel 8031 Microprocessor (using one bit of parallel port as serial port)

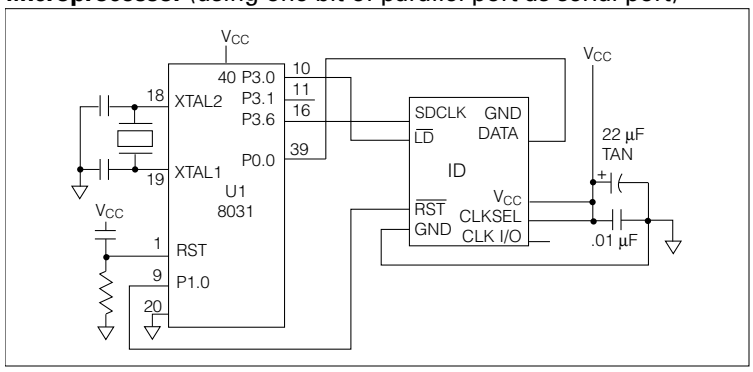


Figure 15. Display Interface with Motorola 68HC05C4 Microprocessor (using SPI port)

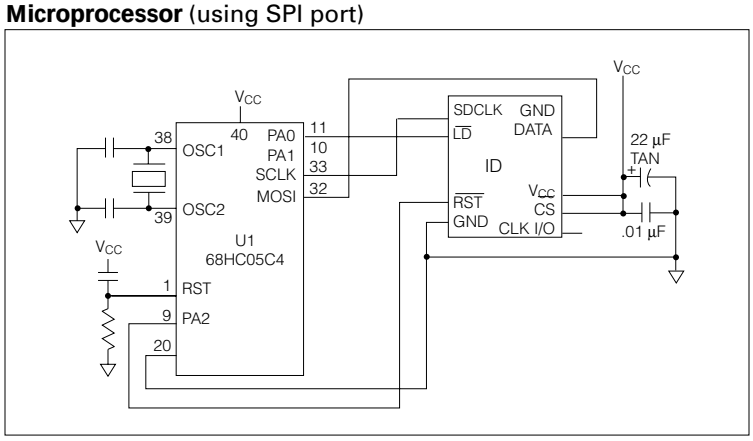
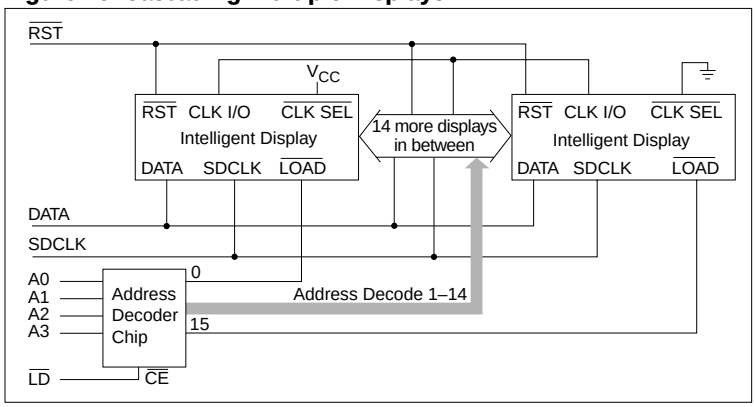


Figure 16. Cascading Multiple Displays



Multiple displays can be cascaded using the $\overline{\text{CLKSEL}}$ and CLK I/O pins (Figure 16). The display designated as the MasterClock source should have its $\overline{\text{CLKSEL}}$ pin tied high and the slaves should have their $\overline{\text{CLKSEL}}$ pins tied low. All CLK I/O pins should be tied together. One display CLK I/O can drive 15 slave CLK I/Os. Use $\overline{\text{RST}}$ to synchronize all display counters.

Figure 17. Character Set